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Research and Development on Advanced Silicon Carbide Thin Film Growth Techniques and Fabrication of High Power and Microwave Frequency Silicon Carbide-Based Device Structures

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Robert F. Davis, R. J. Trew
John W. Palmour, Larry Rowland, Lisa Spellman
c/o Materials Science and Engineering Department
North Carolina State University
Campus Box 7907
Raleigh, NC 27695-7907

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Robert F. Davis

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North Carolina State University
Hillsborough Street
Raleigh,NC 27695

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13. ABSTRACT *(Maximum 200 words)*

The RF operation of MESFETs and bipolar transistors fabricated from both α- and β-SiC have been modeled. The results show that SiC has considerable promise for producing microwave power MESFETs with RF output power capability greater (≈ 4 times) than can be obtained with any of the commonly used semiconductors (e.g., GaAs). This is due to the high breakdown field of SiC that allows high bias voltage to be applied. These device modeling efforts have been used as a guide to design a new MESFET mask set with a aS micron gate length and reduced gate pad area. For the first time, positive gain was observed for a SiC transistor at microwave frequencies. The highest values for F_t and F_{max} were 2.9 GHz and 1.9 GHz, respectively. The highest current and power gains observed at 1.0 GHz were 8.5 dB and 7 dB, respectively. Avalanche characteristics for a 6H-SiC IMPATT were observed for the first time. Heteroepitaxial growth of Ti on (0001) 6H-SiC has been achieved at room and elevated temperatures. Current voltage measurements display shifts toward ohmic behavior after annealing at 400°C. Molecular beam epitaxy equipment has been designed and commissioned.

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I. Introduction

The SiC polytype that currently shows the most promise for high power microwave performance is 6H-SiC. The reason for this choice lies in the high quality and availability of this material more than in its basic electrical properties. For instance, an IMPATT diode relies on operation of a diode in avalanche; while very good avalanche characteristics can now be attained with pn junction diodes in 6H-SiC, no avalanche characteristics have been reported for β-SiC diodes. Likewise, no stable MESFET characteristics have been reported for β-SiC for drain voltages higher than 10 V, while 6H-SiC MESFETs are capable of withstanding drain voltages as high as 100 V. The ability to operate at these higher fields is key to the success of SiC at high frequencies. Because of the excellent crystal quality of 6H-SiC currently being produced by Cree Research, devices fabricated from this material can operate reliably in these high fields.

In order to investigate the suitability of SiC for use in fabrication of high frequency electronic devices, various device types are being modeled in this research program. This investigation is expected to provide guidance regarding device structures most suitable for implementation in this material. Devices currently under consideration include the MESFET, IMPATT diode and Bipolar Transistor. These devices are commonly fabricated from Si and GaAs and are used at microwave and mm-wave frequencies. The material parameters of SiC indicate that this material may allow devices with improved performance to be fabricated. Devices with improved RF output power, in particular, may be possible in SiC.

To achieve the aforementioned devices, as well as other device structures, such that they are operable at or near their theoretical capacity, it will be necessary to improve the ohmic and Schottky contacts to the material and to understand the fundamental science underlying the nature of the interface and its relationship to the electrical properties. A limiting factor in improving performance of SiC based devices is the ability to control the electrical characteristics of metal/SiC contacts. An ohmic

contact, characterized by a low contact resistance and a linear current-voltage relationship, generally is more difficult to obtain due to the need to effectively eliminate any barrier to electron transport. For good rectification properties a large potential barrier between the metal and the semiconductor is desired.

As the above challenges to the advancement of the existing technological base of electronic SiC are being investigated, it is necessary to advance the state-of-the-art, especially in the area of low temperature growth of more perfect thin films. To this end a molecular beam/atomic layer epitaxy (MBE/ALE) system for growth of SiC films by the technique of gas-source molecular beam epitaxy has been designed, purchased, and is currently nearing completion. This deposition system will be used for low temperature growth of monocrystalline SiC thin films, and eventually SiC/AlN solid solutions and SiC/AlN heterostructures.

In this reporting period the RF operation of MESFETs and bipolar transistors fabricated from both alpha-and beta-SiC have been modeled. These device modeling efforts have been used as a guide to design a new MESFET mask set having submicron gate lengths and reduced gate pad area. For the first time, positive gain was observed for a SiC transistor at microwave frequencies. Avalanche characteristics for a SiC IMPATT were also observed for the first time. In addition heteroepitaxial growth of Ti on (0001) 6H-SiC has been achieved at room and elevated temperatures. Finally molecular beam epitaxy equipment for the thin film growth of SiC has been designed, fabricated and commissioned. The details of this research as well as future plans are given in the following sections.

II. Modeling and Characterization of Electronic Devices Fabricated from SiC (Trew-NCSU)

A. Overview

The device simulation effort is directed towards investigation of the RF potential of various types of electronic device structures fabricated in SiC. The goals

are to simulate the operation of the various devices under realistic operation conditions and to compare their RF performance to comparable devices fabricated from more commonly used semiconductors such as Si and GaAs. In this manner, specific devices most suitable for fabrication in SiC can be identified.

The experimental characterization effort supports both the simulator development effort and the device fabrication work. Prototype devices have been fabricated and tested to determine the dc and RF characteristics. The measured data has been compared to the simulated results to verify the models and to provide direction as to important physical effects that need to be modeled. The feedback allows improvements to be made, thereby permitting accurate, advanced device models to be developed. The models are then used to provide guidance for improved device designs.

B. Procedures

Theoretical models for various types of electronic devices are being developed. The work has so far concentrated upon MESFET and IMPATT models developed at NCSU and models for bipolar transistors available in commercial RF simulators. Improved accuracy bipolar models are currently under development at NCSU. The models are being improved by the addition of physical effects found to be of importance. The model enhancement work has so far involved the development of algorithms for thermal effects, breakdown phenomena, and parasitic elements. The additional features are being incorporated into the basic device simulators.

A characterization procedure for investigating the RF performance of prototype MESFET devices is being developed. The characterization facility allows dc, microwave (currently up to 26.5 GHz), thermal, and parasitic measurements to be performed using an on-wafer procedure.

C. Results

The RF operation of MESFETs and bipolar transistors fabricated from both α-Si and β-SiC has been investigated. Typical device structures have been designed,

optimized, and their RF performance simulated. The relatively low electron mobility of α-SiC and the extremely low hole mobility of this material limit its use for fabricating high performance microwave bipolar transistors. It is unlikely that SiC BJTs will perform well above 3 GHz. However, below this frequency SiC BJTs are capable of producing significant RF output power which is greater than is available from similar Si transistors.

SiC MESFETs with good microwave characteristics, especially RF output power are also possible. In order to obtain maximum RF output power these devices are scaled to the greatest width possible. This, in turn, minimizes the degrading effects of low electron mobility. Also, since these devices use only majority carriers (electrons in this case) the device does not require any p-type material.

Simulations of the RF performance of SiC MESFETs designed to operate at 10 GHz were performed. A cross-section of the device is shown in Figure 1 and the parameter values used in the simulation are presented in Table I. Devices with gate lengths of 0.5 and 1 μm were investigated. The gate width was 1 mm. These dimensions are typical of those used to fabricate GaAs microwave MESFETs. The material parameters listed in Table I are typical of currently available α-SiC.

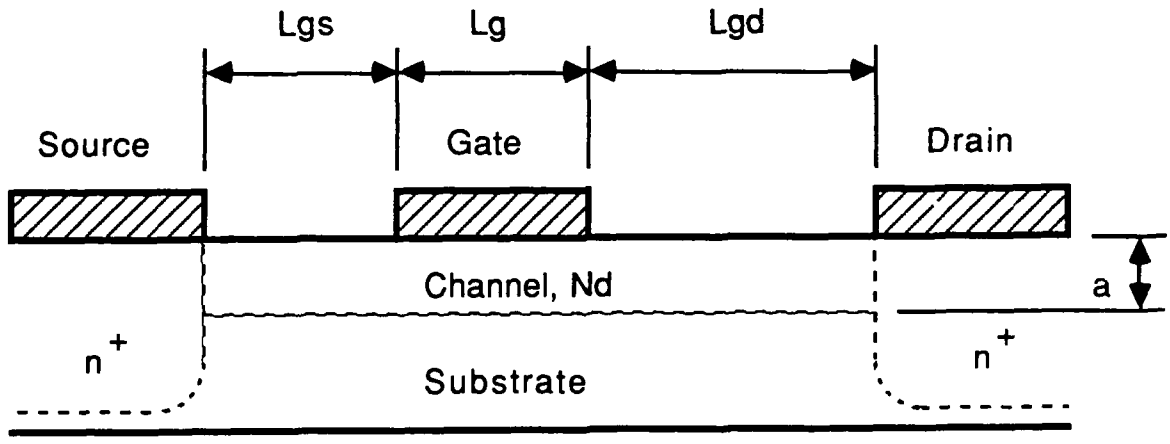

Figure. 1 Cross-section view of a SiC MESFET.

Table I. Parameter values used in the SiC MESFET simulation

Parameter	Value
L_g	0.5, 1.0 μm
W	1 mm
N_d	2.4×10^{17} cm^{-3}
a	0.25 μm
L_{gd}	2 μm
L_{gs}	1 μm
μ_n	240 cm^2/V-sec
v_s	2×10^7 cm/sec
ε_r	10
V_{bi}	1.95 V
V_{dsbd}	83
θ	5°K/W
R_c	10^{-5} Ω–cm^2

The dc I-V characteristics for the 0.5 μm and 1 μm gate length devices are shown in Figures 2 and 3, respectively. The 0.5 μm and 1 μm gate length devices produce a maximum channel current of about 490 mA and 330 mA, respectively. The increased channel current from the shorter gate length MESFET is due to a higher electric field in the conducting channel. The increased electric field results in increased electron velocity and the observed increase in channel current. The pinch-off voltages for the devices are –11.6 V and –11.7 V. The RF performance for the two devices biased for class A operation is compared in Figures 4, 5 and 6. The drain bias was set to Vds = 40 V and the channel current was set to Ids = Idss/2. The RF output power versus RF input power is shown in Figure 4. Both devices go into saturation at an input power level of about 25 dbm. The 0.5 μm and 1 μm gate length devices produce 37 dbm (Po = 5.0 W/mm) and 35.3 dbm (Po = 3.39 W/mm), respectively. These numbers compare favorably with the approximately 1 W/mm RF power obtainable from similar GaAs microwave power MESFETs. Good power-added efficiency can

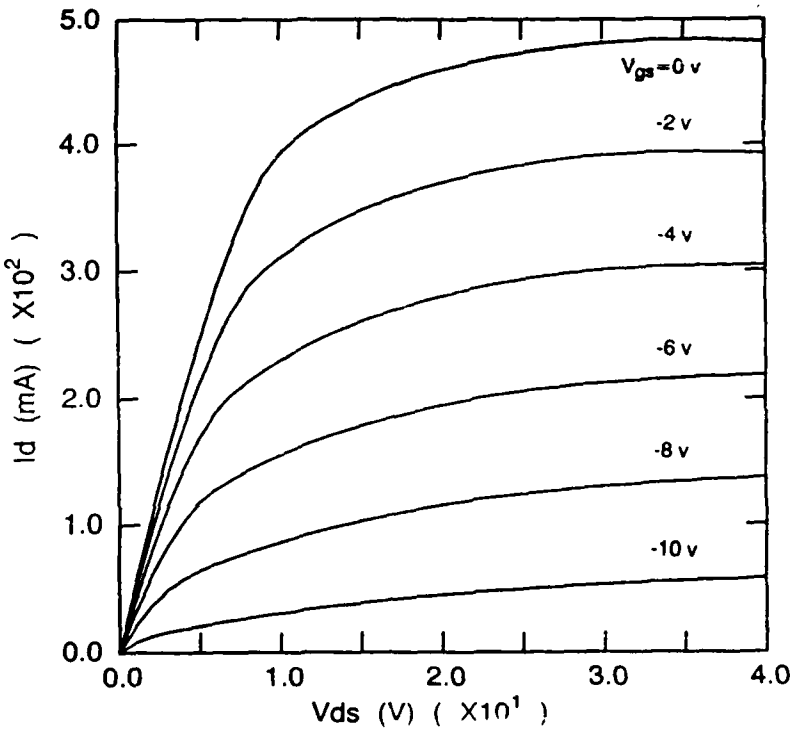

Figure 2. dc I-V characteristics for a 0.5 μm gate length SiC MESFET (W = 1 mm).

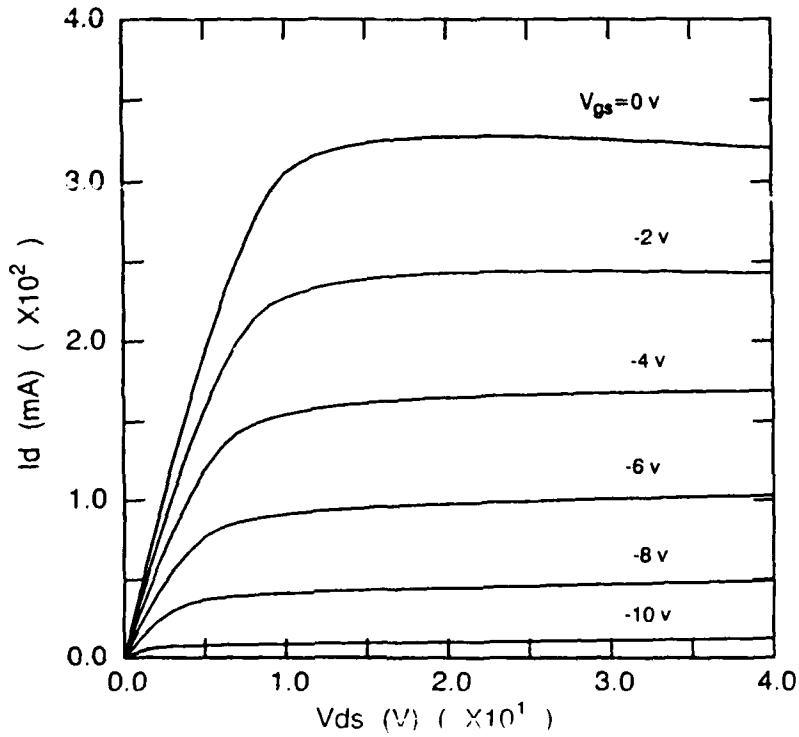

Figure 3. dc I-V characteristics for a 1.0 μm gate length SiC MESFET (W = 1 mm).

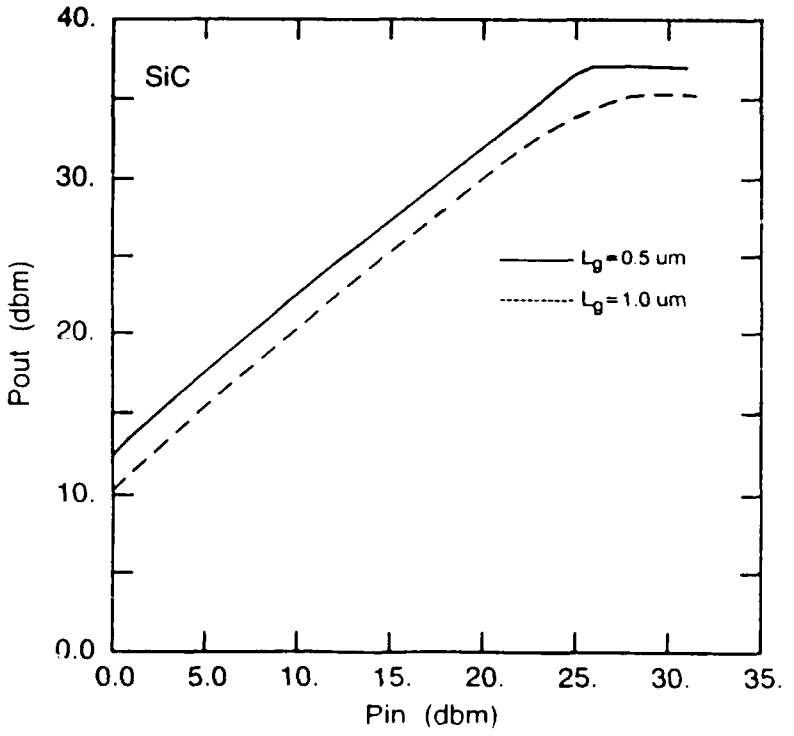

Figure 4. RF output power vs. input power at 10 GHz for the SiC MESFET (W = 1 mm, Vds = 40 V, Ids = Idss/2).

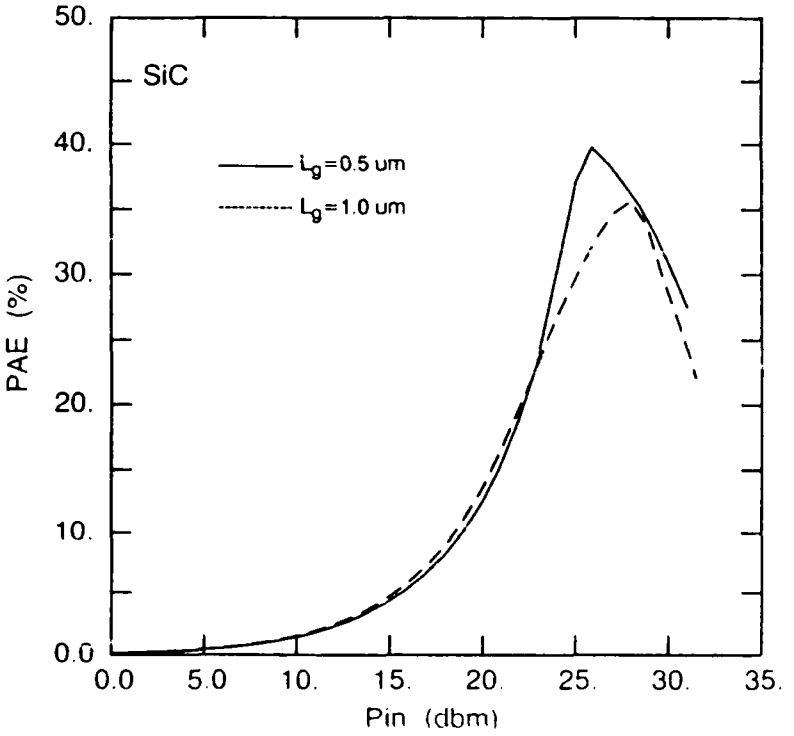

Figure 5. Power-added efficiency vs. input power at 10 GHz for the SiC MESFET (W = 1 mm, Vds = 40 V, Ids = Idss/2).

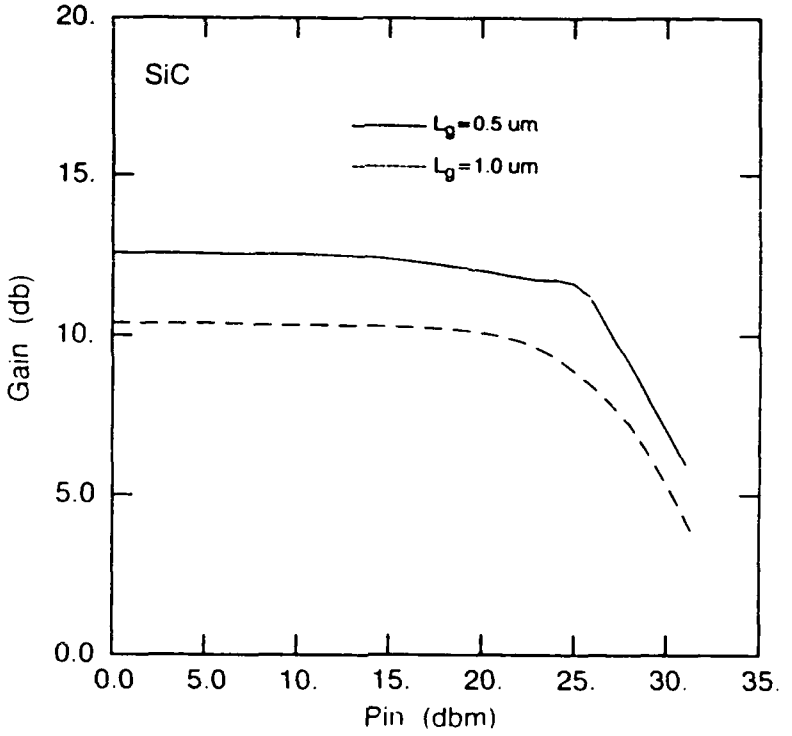

Figure 6. Gain vs. input power at 10 GHz for the SiC MESFET (W = 1 mm, Vds = 40 V, Ids = Idss/2).

also be obtained as indicated in Fig. 5. The 0.5 μm and 1 μm gate length devices produce maximum PAE of 40% and 36%, respectively. The gain versus input power for the two devices is shown in Figure 6. The 0.5 μm and 1 μm gate length devices produce 12.5 db and 10.4 db linear gain, respectively.

D. Discussion

The results of the simulations indicate that SiC has considerable promise for producing microwave power MESFETs with RF output power capability greater than can be obtained with any of the commonly used semiconductors. A properly designed and fabricated SiC MESFET should be capable of producing about 4 times the microwave RF output power obtainable from a comparable GaAs MESFET. The improved RF output power capability of the SiC device is due to the high breakdown field of SiC that allows high bias voltage to be applied. This, in turn, allows charge carrier saturation to occur in the conducting channel, thereby minimizing the effects of low carrier mobility. Operating the channel under the gate region in saturation allows

the device to make use of the high electron velocity offered by SiC. This, in turn, results in maximized channel current and a corresponding high RF output power.

Gate-drain breakdown is also key to obtaining high RF output power since achieving saturation conditions requires high drain bias to be applied. The calculations reported here assumed that the high critical field for breakdown in SiC could be utilized. Work on MESFETs, however, often indicates high gate leakage currents, the reason for which is not currently understood. The high gate leakage is observed in MESFETs fabricated from all semiconductor materials. Recently, a theory of gate breakdown in MESFETs has been formulated at NCSU. According to this theory, gate leakage is due to a surface conduction mechanism. Charge carriers travel from the gate metal to the drain electrode by means of a surface trap hopping mechanism. Suppression of this surface conduction mechanism should block the gate leakage and allow high drain bias to be applied.

The gate breakdown formulation will be continued during the next reporting period and explicitly applied to SiC MESFETs. It is anticipated that this work will result in design techniques for reducing the high gate leakage currents.

III. Fabrication and Characterization of SiC Devices for Microwave Applications (Palmour-Cree Research, Inc.)

A. Overview

High frequency MESFET devices have been reported in previous progress reports for this contract. In the last report, the effect of gate resistance as a major parasitic for high frequency operation was discussed. Preliminary experiments showed that a large increase in F_{max} resulted from using a 200 nm thick overlayer of Al on top of the gate contact. The best values of F_t and F_{max} that were reported using this overlayer were 1.6 GHz and 770 MHz, respectively. At 500 MHz, the device had a power gain of 4.6 dB and a current gain of 8.5 dB. It was predicted at that time that further improvements in gate resistance would result in even higher frequency operation.

The devices discussed above were the last ones fabricated using the original MESFET mask set designed for this project. The gate lengths were generally no shorter than 1.8 μm using this mask set and the contact printing lithography available at that time. Therefore it was also predicted that the high frequency behavior would improve greatly when smaller gate lengths were acheived using a newly designed mask set. Although it was not considered to be a major parasitic, the gate capacitance was also higher than desired, due primarily to the gate contact pad. Of the measured 5.75 pF of gate capacitance, only 1.7 pF was due to the Schottky gate contact, with the other 4 pF arising from the 300 nm thick Si_3N_4 isolation pad.

The main focus of this reporting period has been to confirm the high power/high frequency behavior of 6H-SiC by fabricating high power MESFET structures using a newly designed mask set. The primary objective has been to identify and eliminate the parasitic resistances and capacitances of these devices in a systematic way, using the device modeling efforts as a guide, so that each batch of devices can show an incremental increase in high frequency performance. These improvements encompassed both fabrication procedures and device design, and have resulted in significant improvements in the high frequency characteristics of 6H-SiC MESFETs.

The other high frequency device that has been investigated is the IMPATT diode. The last report discussed the problems associated with fabricating the normal "flat" profile IMPATT diodes without getting very high leakage currents. The leakage currents arose from an inherent passivation problem for the 6H-SiC at the high voltages (400-500 V) required for the "flat" profile IMPATTs. Thus it was proposed that future IMPATT diodes would be fabricated using a "high-low" doping structure that would allow low voltage avalanche to occur in a heavily doped region and the avalanche current would then go through a lower doped drift region. These "high-low" structures were fabricated during this reporting period using both a pn junction diode and a Schottky diode. While no high frequency characteristics have been measured for these devices, the combination of results achieved during this period are promising.

B. Experimental Procedure

High Power/High Frequency MESFETs. The substrates used for this study were sliced from 6H-SiC single crystal boules. The boules were lightly nitrogen doped and n-type. The boules were sliced, lapped and polished into wafers suitable for epitaxial growth. Thin films of monocrystalline 6H-SiC (0001), both p- and n-type, were epitaxially grown on these n-type 6H-SiC (0001) wafers. The MESFET, shown in cross-section in Figure 7, consisted of a 2 μm thick p-type expitaxial layer of 6H-SiC having a carrier concentration in the range of $1\text{-}2\text{x}10^{16}$ cm^{-3} grown on the n-type 6H-SiC substrate. This p-type layer acted as the buried layer to confine the current to a thin n-type active region which was subsequently grown. This top epitaxial layer had carrier concentrations in the range of $6\text{x}10^{16}$ cm^{-3} to $1.5\text{x}10^{17}$ cm^{-3} and a thickness of 0.25 to 0.34 μm depending on the doping and desired pinch-off voltage of the device. The formation of the ion implanted wells, ohmic contacts, and Schottky contacts on the channel layer is discussed later.

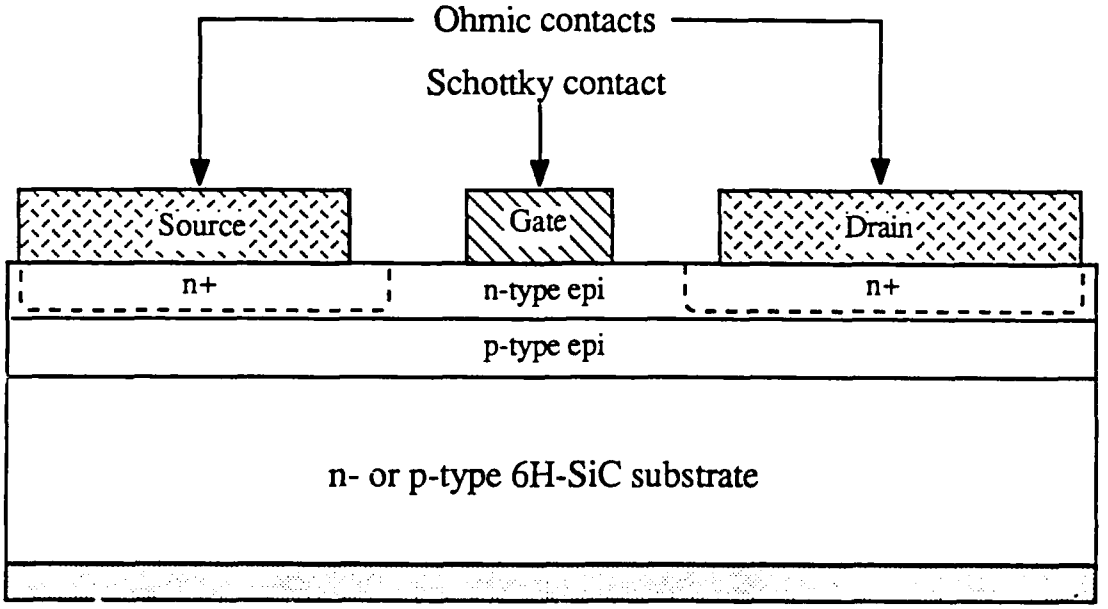

Figure 7: Cross-sectional view of 6H-SiC MESFET design utilizing ion implanted n^+ source and drain wells, and a buried p-type isolation layer.

The new design for the high power-high frequency SiC MESFET is shown in Figure 8. This design still uses a 1 mm gate width consisting of two 500 μm long gate

fingers, but it uses much smaller source and drain ohmic contact areas that make the overall device size 27% smaller. The smaller contact area was allowed because of the n^+ source and drain implants that were used, as opposed to the previous design. Shorter gate lengths were used on this mask, varying from 0.6 μm to 1.0 μm. The gate - drain spacing was increased from 1 μm to 1.5 μm to allow higher drain voltages to be attained. The source - gate spacing was 1 μm (accounting for gate line spread) for all of the devices except the smallest gate length, which had a 0.5 μm spacing. To further reduce the gate capacitance, the gate contact pad area was reduced to the minimum value that still allows reliable wire bonding. Finally, source and drain metal overlayers were used to facilitate better contacting for probing as well as wire bonding.

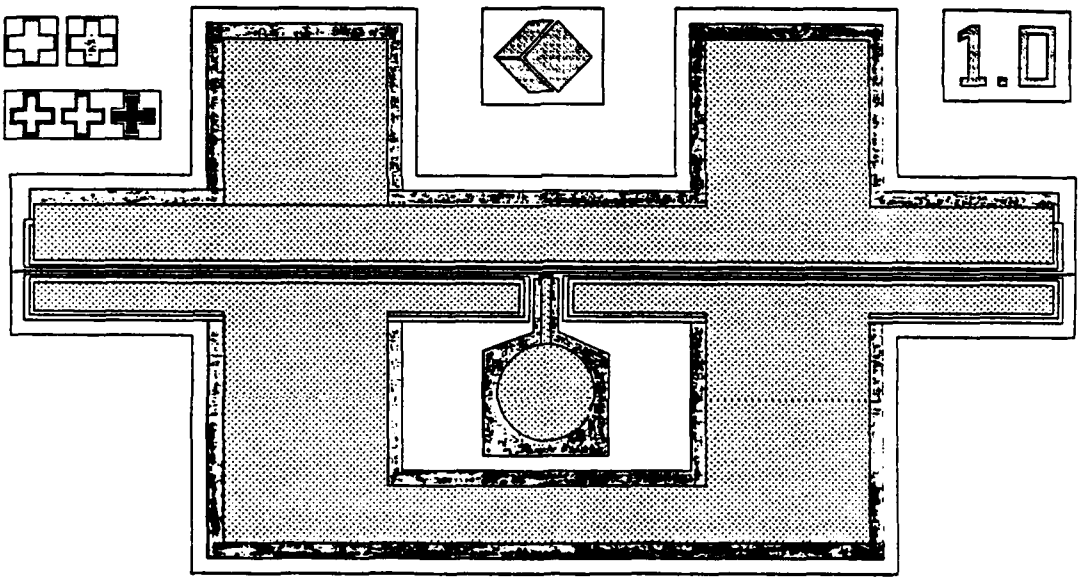

Figure 8. New design for high power, high frequency SiC MESFET. Gate lengths vary from 1.0 μm to 0.6 μm, and source-to-drain distances vary from 3.5 μm to 2.9 μm. The gate width is 1 mm.

The fabrication of these devices was as follows. The entire device was first isolated on a mesa. Using conventional photolithography techniques, a sputtered aluminum film was patterned onto the SiC surface, which acted as a mask for the reactive ion etching of the isolation mesa. The material around the mesa was etched sufficiently deeply enough to penetrate through the top n-type layer into the buried

p-type layer. The Al was then stripped, and polysilicon was deposited and patterned, opening windows for the source and drain pattern. The samples were then ion implanted with N^+ to form n^+ source and drain wells, using the polysilicon as the implant mask. The implants were subsequently annealed and the samples oxidized to grow a thin passivating layer of SiO_2. A 500 nm thick layer of SiO_2 was then deposited, using a low temperature chemical vapor deposition process, over the thin thermal oxide. This layer was patterned to form the center gate contact isolation pad and interconnect bars. Windows for the source and drain contacts were then opened in the SiO_2, and the ohmic contacts were deposited and patterned using the "lift-off" technique. After these ohmic contacts were annealed, the fine line gate Schottky contact with overlayer was patterned using an excimer laser stepper. Finally, the gate contact pad metallization was deposited and patterned on the SiO_2 isolation pad.

One of the key steps in this process scheme was the gate lithography. A process was developed for achieving fine line lithography on SiC wafers using a GCA ALS LaserStep 200 (an excimer laser stepper) at the Microelectronics Center of North Carolina on a subcontract basis. This process, which used Shipley 8843-I deep UV photoresist, resulted in much improved fine line lithography that allowed gate lengths as small as 0.6 μm to be developed. The characteristics of these fine line devices will be discussed in Section C–Results and Discussion.

Some of the devices utilized a mesa source and drain structure rather than using ion implantation. After epitaxial growth of the n-type channel layer, another n-type layer with heavy nitrogen doping was grown on top. This layer typically had a thickness of 0.2 μm and a doping of $1x10^{19}$ cm^{-3}. The source and drain were defined by reactive ion etching the n^+ layer away except where the source and drain contacts were to go, using the same mask as was used for the ion implants. The insulator layers and gate contacts were then deposited on the etched back channel layer, just as was done for the devices previously discussed.

IMPATT Diodes. All of the IMPATT diodes that were fabricated during this

reporting period used the "high-low" design for low voltage avalanche. Both pn junction and Schottky diode structures were made. Both structures had the same epitaxy for the breakdown layers, as is shown in Figure 9. The starting substrates were n-type that were doped with nitrogen so that n = 1-3x10^{18} cm^{-3}. The first epilayer, which serves as the drift layer, was then grown with a thickness of 1.2 μm and a carrier concentration of 3-4x10^{16} cm^{-3}. This layer was followed by a more heavily doped avalanche layer with a thickness of 0.22 μm and carrier concentration of 3-5x10^{17} cm^{-3}. The samples for the Schottky diode IMPATTs were then ready for processing. The pn junction IMPATT wafers had a subsequent p^+ layer grown on them that was 0.8 μm thick and had a carrier concentration of p = 3-5x10^{18} cm^{-3}.

The device fabrication for the IMPATT diodes involved first thining the wafers to 125 μm thick by diamond grinding the backside of the wafer. The diode mesas were then formed via reactive ion etching using Al as the mask material. The mesas were etched through the epilayers into the n^+ substrate. The samples were then oxidized in dry O_2 to form a passivating layer of oxide on the mesa sidewalls. Using photolithography, windows were etched in the oxide for the topside Schottky or ohmic contacts, depending on whether the wafers were Schottky or pn junction IMPATTs, respectively. The topside contacts were then formed on the front and backside of the wafer as shown in Figure 9. The one difference is that the backside via shown in Figure 9 was not fabricated because of the difficulty in handling the very thin wafers. When the optimal device structure is determined, future devices will have these backside vias etched in them. The reason for these vias is to reduce the substrate resistance, allowing higher frequency operation. Ideally, this via would be etched as deep as 100 μm, giving a 25 μm distance from the drift layer to the ohmic contact. In practice, the etch depth will probably be in the range of 25-50 μm because of wafer breakage problems. The same set of masks were used for both Schottky and pn junction IMPATTs. Seven different diameter dots, varying from 38.1 μm to 381 μm, were used in order to find the device area that yielded the best impedance matching.

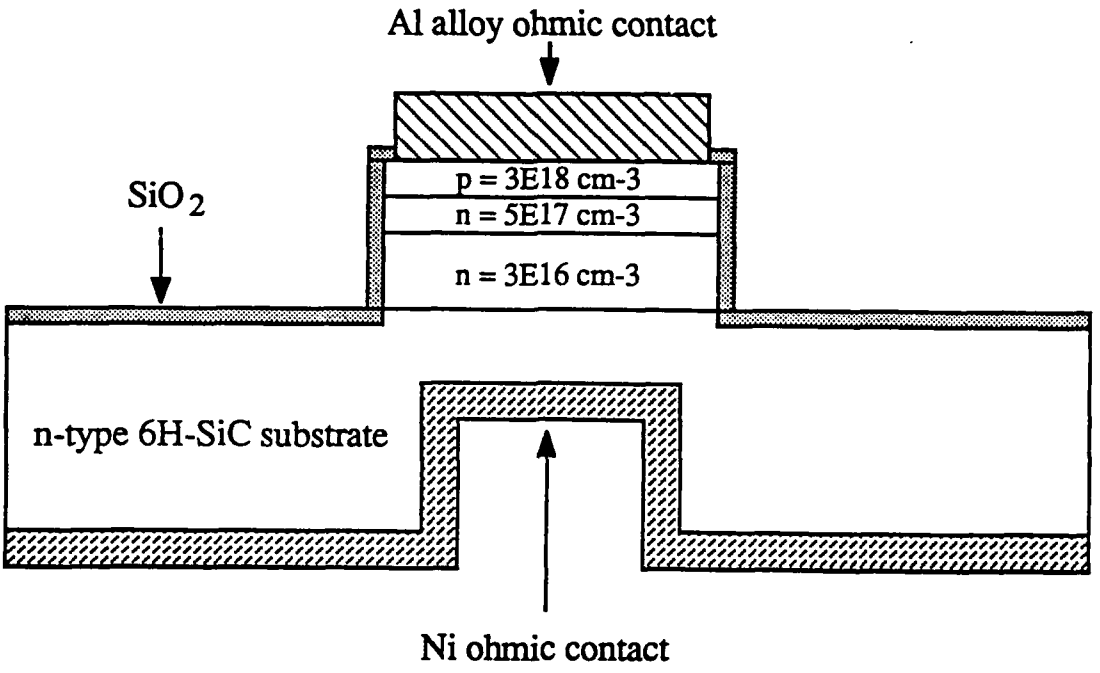

Figure 9. Cross-sectional view of pn junction "high-low" IMPATT diode structure in 6H-SiC. Schottky "high-low" IMPATTs have same structure except there is no p^+ layer on top and top contact is a Schottky instead of an ohmic.

C. Results and Discussion

High Power/High Frequency MESFETs. Four batches of high frequency MESFETs were finished in this reporting period. The first two were fabricated using the old mask set and Si_3N_4 isolation pads that have been described in previous reports. The efforts on those devices were mainly focused on achieving thicker gate overlayers to reduce the gate resistance. While these efforts did increase the high frequency parameters somewhat, the bulk of the progress made was with the devices fabricated using the new design.

As was described earlier, the new design used a deposited SiO_2 for the pad isolation to achieve lower gate capacitances and utilized an excimer laser stepper to achieve much shorter gate lengths on the devices. These efforts were very successful in those two areas. In terms of parasitic gate capacitance, the value was reduced from 5.75 pF to 1.9 pF. This was due to the smaller area gate contact pad and the use of deposited SiO_2 as the pad isolation material. The SiO_2 was used because of its low

dielectric constant of 3.9 as compared with that of Si_3N_4 (7.5), which was used in earlier devices.

Using the excimer laser stepper, sub-micron lines were achieved for the first time in SiC. The minimum gate length acheived was between 0.6 and 0.7 μm (the intended gate length was 0.6 μm). The smallest gate length that had been achieved previously was about 1.7 μm. Furthermore, overlayers of gold as thick as 750 nm were deposited on top of the gates. The laser stepper also allowed a much higher yield of devices per wafer.

A typical DC current-voltage plot of one of these 6H-SiC MESFETs fabricated with the new mask is shown in Figure 10. This device had a gate length and width of 0.7 μm and 1 mm, respectively. Although this device had a breakdown voltage at V_D = 14 V, other devices demonstrated drain voltages as high as 45 V. The maximum transconductance of this device was 25 mS/mm at V_D = 20 V and V_G = 0 V, and the measured channel resistance was 39 Ω. The pinch-off voltage was at V_G = -8.5 V. The gate leakage at V_G = -1.5 V and V_D = 14 V was 363 μA, but increased to 5 mA at V_G = -9 V and V_D = 14 V, which is quite high. This device had a 600 nm thick gold overlayer on the gate.

The positive benefits of the reduced gate length were made apparent by measurement of the 6H-SiC MESFETs at high frequency. This device was measured at high frequency using an HP 8510 automatic network analyzer with a Cascade Microprober for standard S-parameter measurements. The plot in Figure 11 shows that this device has a threshold frequency (F_t) of at least 2.9 GHz. Although the H_{21} parameter actually crosses 0 dB gain at 3.5 GHz, there is some curvature to the slope that makes this value unreliable. Therefore, the value of F_t =2.9 GHz was derived by extrapolation of the lower frequency data. The device has an F_{max} of 1.8 GHz, where the power gain (G_{max}) crosses 0 dB gain. The previously observed average values for F_t and F_{max} were 1.6 GHz and 770 MHz, respectively.

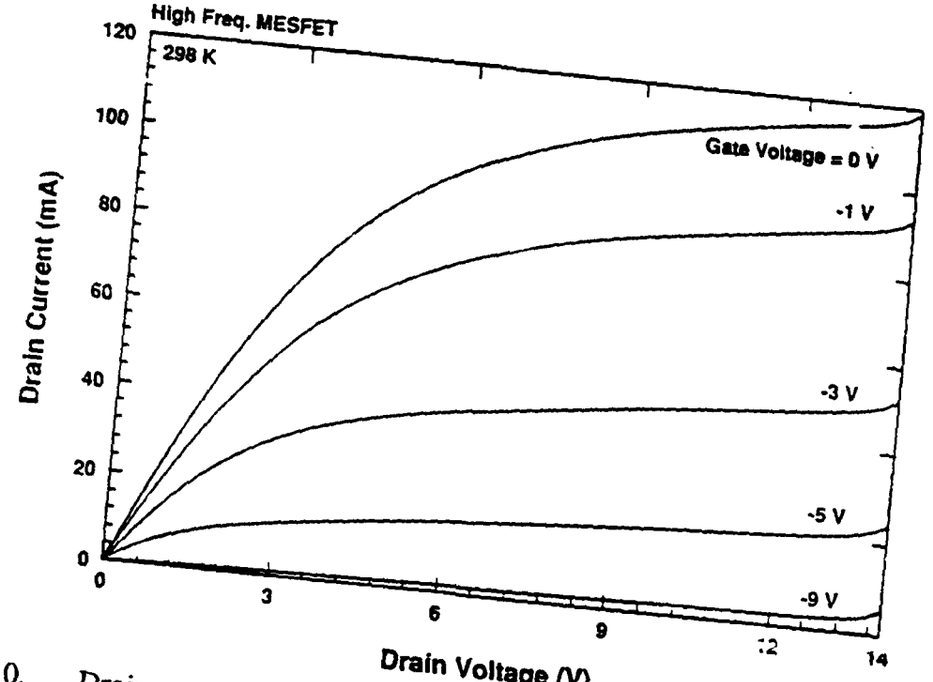

Figure 10. Drain current-voltage characteristics of a SiC MESFET using the design shown in Fig. 8. Gate length and width were 0.7 μm and 1 mm, respectively. Source-drain distance was 2.1 μm. The maximum transconductance was 25 mS/mm.

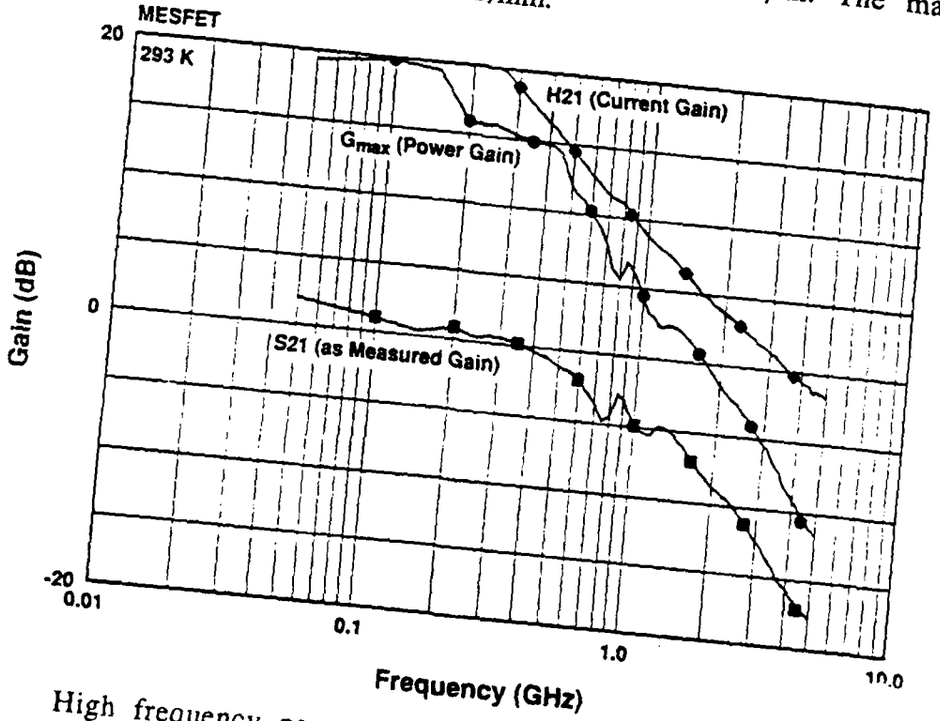

Figure 11. High frequency parameters, S_{21}, G_{max}, and H_{21}, as a function of frequency for the 0.7 μm gate length device shown in Figure 10. Measurement conditions were V_D = 14 V, I_D = 81 mA, V_G = -1.5 V, and I_G = 363 μA.

The DC current-voltage plot in Figure 12 shows another 6H-SiC MESFET device that has higher drain voltage capability. This device also had a gate length and width of 0.7 μm and 1 mm, but it had a thicker gold overlayer of 750 nm. This device showed good current saturation out to 35 V and a non-destructive breakdown of the SiC at V_D = 37 V. The maximum current for this device was only 50 mA because the channel thickness was not as thick as it should have been, as evidenced by the pinch-off voltage of V_G = -4.5 V and the measured source-drain resistance of 67 Ω. The maximum transconductance of this device was 19 mS/mm at V_G = 0 V. The gate leakage current at V_G = 0 V and V_D = 33 V was 385 μA, and increased to 800 μA at V_G = -4.5 V.

A gain vs. frequency plot for the same device with the 750 nm overlayer shown in Figure 12 is shown in Figure 13. As was expected, the F_t of 2.4 GHz was lower than the previously discussed device because of the much higher source-drain resistance. However, despite the higher resistance, the F_{max} of 1.9 GHz was even higher than the previous device. It is proposed that the thicker gate overlayer (25% thicker) caused sufficient drop in the parasitic gate resistance to overcome the effects of the higher source-drain resistance. At 1.0 GHz, the device in Figure 11 had a power gain of about 4.5 dB and a current gain of 8.5 dB. The device in Figure 13 with reduced gate resistance had a power gain and a current gain of 7.0 dB each at 1.0 GHz. Based on these results, it is apparent that the gate resistance is by far the most important parasitic to be addressed.

While these are marked improvements in high frequency operation, they are somewhat lower than first expected, since the gate lengths were reduced by almost 60% over devices that were fabricated in previous batches. However, for every reduction in gate length, there must be an equivalent increase in gate overlayer thickness to maintain the same cross-sectional area and same gate resistance. The gates of these devices are still not thick enough at 750 nm. Given the very small cross-section and the long finger length (500 μm), the series resistance along the gate

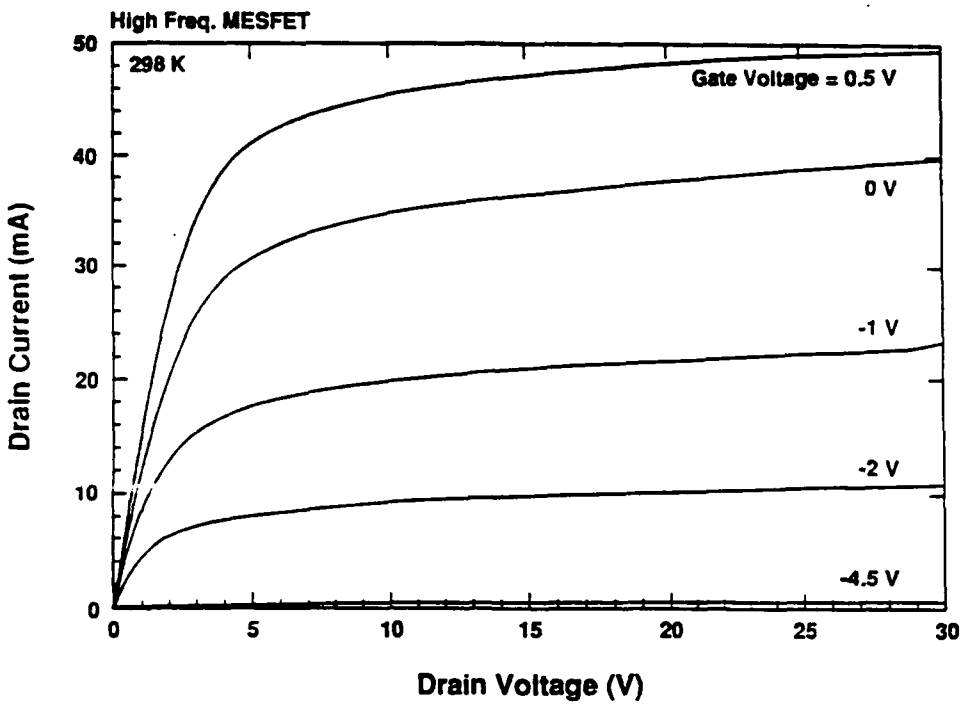

Figure 12. Drain current-voltage characteristics of a 6H-SiC MESFET with a thicker gold gate overlayer (750 nm). Gate length and width were 0.7 μm and 1 mm, respectively. Source-drain distance was 2.1 μm. The maximum transconductance was 19 mS/mm.

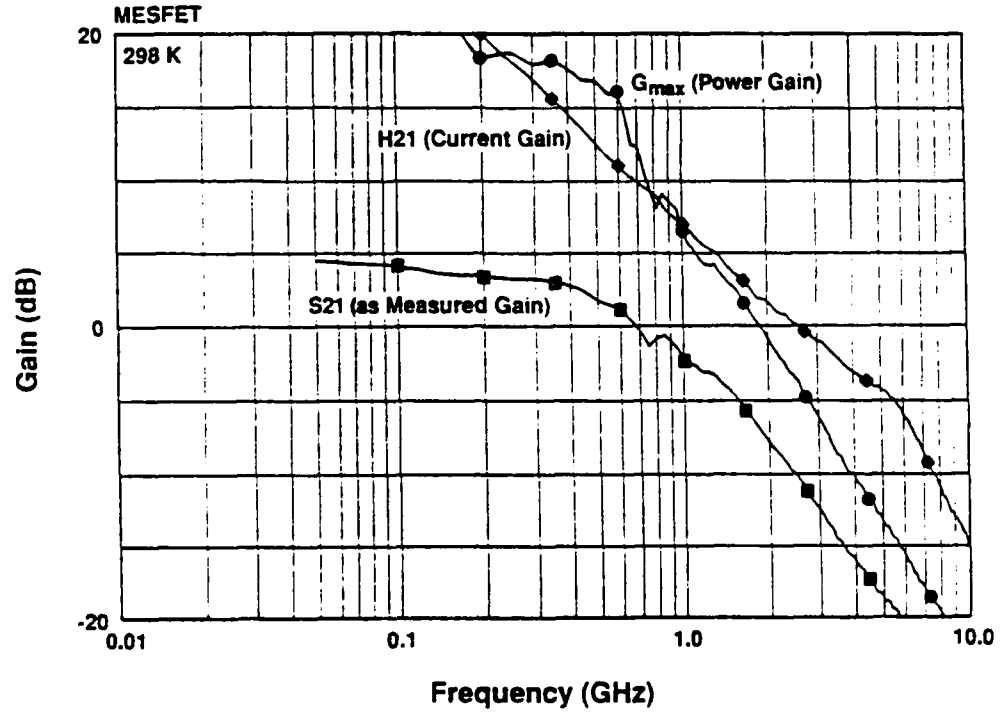

Figure 13. High frequency parameters, S_{21}, G_{max}, and H_{21}, as a function of frequency for the device shown in Figure 12. Measurement conditions were V_D = 33 V, I_D = 50 mA, V_G = 0 V, and I_G = 385 μA.

fingers still have values in the range of 35-40 Ω. For GaAs MESFETs, it has been found that 10 Ω of gate resistance is a "critical" value to avoid serious parasitic effects, with a preferred value of 1.5 Ω. These low values of gate resistance are achieved by using thick overlayers of gold on top of the gate contacts, quite often employing techniques that enlarge the cross-sectional area (mushroom gates). As such, future efforts for 6H-SiC MESFETs will be to further reduce the parasitic gate resistance. Device modeling of the effects of gate resistance on the high frequency performance of 6H-SiC MESFETs is further discussed in the Physical Modeling Section of this report.

IMPATT Diodes. The initial modeling for IMPATT diodes was for operation at 60 GHz using a flat profile for the drift layer, and showed that this epilayer must have $n = 4 \times 10^{16}$ cm^{-3} and a thickness of 2 μm. This thickness and carrier concentration are dictated by that desired frequency. However, none of the structures showed promising avalanche characteristics, because of the amount of sub-avalanche reverse bias leakage current due to passivation problems. Most of the devices had a leakage current of about 1 mA at a reverse bias of 30 V, which was well below the avalanche voltage. Therefore, further efforts focused on using a "high-low" structure, which would keep the avalanche voltage low and decrease the sidewall passivation requirements. These "high-low" structures were made using both a pn junction diode and a Schottky diode.

The pn junction high-low IMPATT structures showed very low reverse bias leakage currents as compared with previous devices. Unfortunately, the doping and/or thickness of the avalanche layers were off enough so that avalanche could not be achieved. The I-V characteristics of the pn junction high-low IMPATT diode shown in Figure 14 show that reverse bias voltages of 200 V were achieved with very low leakage current. The average leakage current at V = -200 V was 2-4 μA. Voltages higher than 200 V caused a permanent breakdown phenomenon assumed to be passivation failure. There are two possible reasons these did not avalanche at the

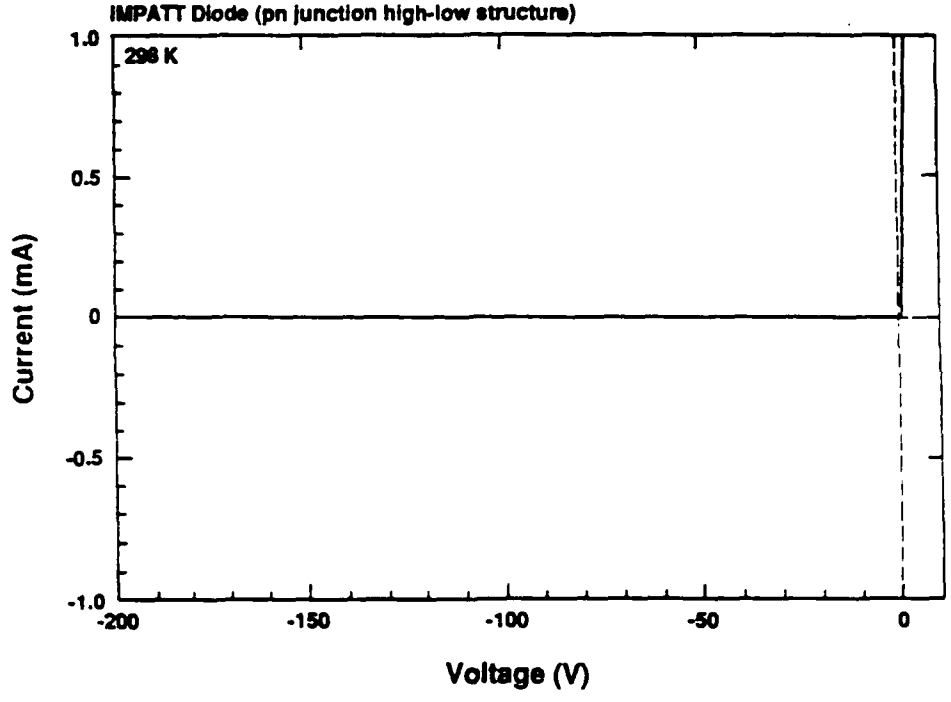

Figure 14. Current-voltage characteristics of a 6H-SiC pn junction "high-low" IMPATT diode structure, as shown in Fig. 9.

expected value of 100 V. The actual carrier concentration of the "high" avalanche layer could have been lower than what was measured, thus requiring a thicker layer and higher voltage. The other reason would be that the avalanche layer thickness could have been thinner than was assumed and the depletion region reached the "low" doped drift layer before the avalanche voltage was achieved, allowing the low doped material to take the rest of the voltage.

While avalanche was not achieved, these are encouraging results. If the doping and thickness had been correct for this device, it is apparent that it would have avalanched at about 100 V with very low sub-avalanche leakage current using this device structure. Therefore, these structures will be further investigated.

The Schottky high-low IMPATT diodes that were fabricated in this study showed the first avalanche characteristics ever observed for a SiC Schottky device. The I-V characteristics shown in Figure 15 show that avalanche was achieved at a voltage of 43 V. Furthermore, the reverse bias leakage current was quite low, with a value of 2 μA at V = -20 V. This device had a diameter of 203 μm, therefore the

leakage current translates to 6 mA/cm^2. The device had a sharp turn-on voltage in forward bias of 0.85 V, and forward current reached 200 mA at 1.9 V, which corresponds to a resistance of 5.25 Ω.

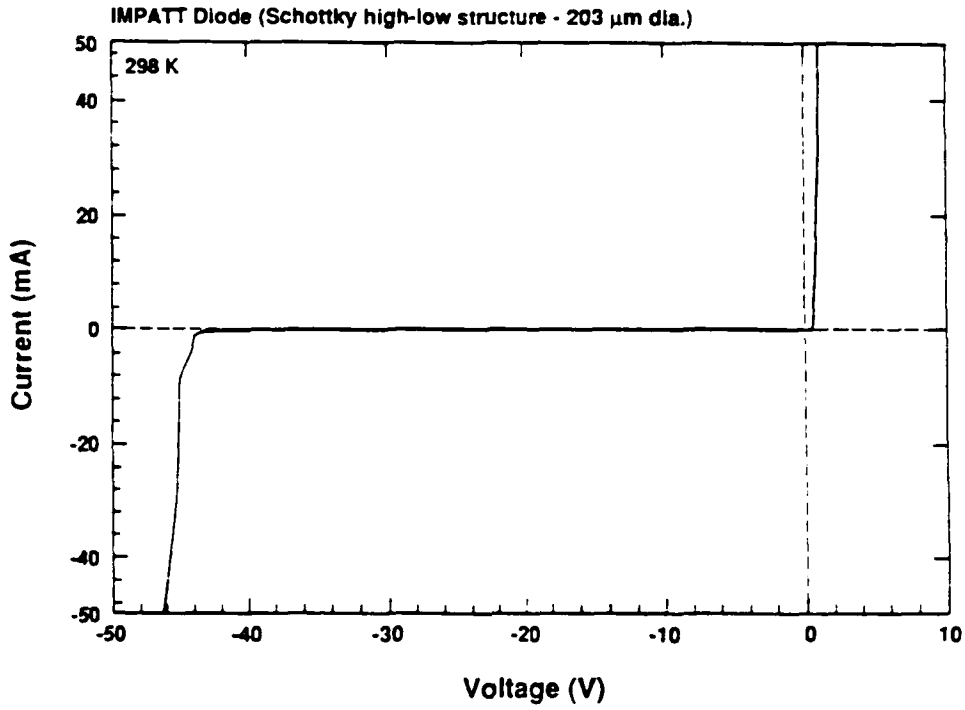

Figure 15. Current-voltage characteristics of a 6H-SiC Schottky barrier "high-low" IMPATT diode structure. Note avalanche current at reverse bias of -44 V.

The avalanche was also relatively sharp and had roughly the same slope as the forward bias current. This device withstood as much as 50 mA in avalanche current at 46 V, corresponding to an avalanche power density of 7.1 kW/cm^2. Another Schottky high-low device with a smaller diameter is shown in Figure 16. This device had a diameter of 102 µm. Although higher leakage current prevents the avalanche and forward turn-on from being as sharp as the previous device, this device does show that a very high avalanche current density can be achieved with 6H-SiC. This device withstood more than 40 mA at 59 V, which corresponds to a very high avalanche power density of 29 kW/cm^2.

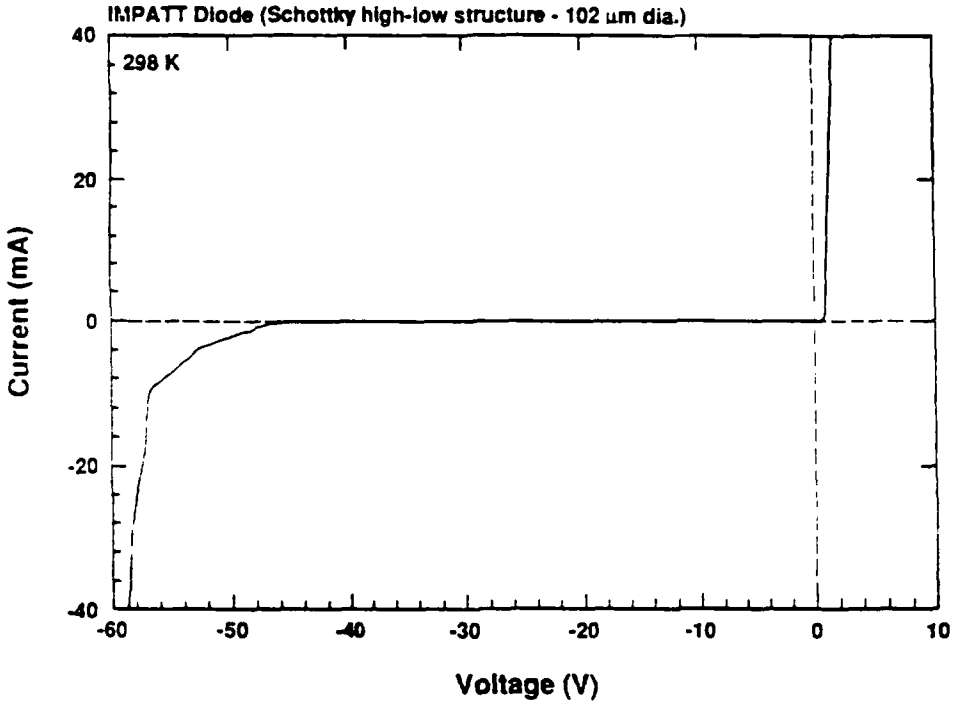

Figure 16. Current-voltage characteristics of 6H-SiC Schottky barrier "high-low" IMPATT diode structure. The avalanche current shown corresponds to a power density of 29 kW/cm^2.

While these Schottky-based IMPATTs seem to be the best structure to date, there is a very fundamental problem observed with these devices that will probably prevent them from being used for 60 GHz operation. The resistances of these diodes ranged from 4-20 Ω depending on the diameter of the device. Using known bulk resistivities and ohmic contact resistivities for 6H-SiC, the contact resistivity of the Schottky contact, an unknown until now, was calculated from the I-V characteristics. In forward bias, it appears that the Schottky contact contributes a contact resitivity of about 8×10^{-4} Ω-cm^2. Although the calculated value is not exact, it is a good estimation of the range of the contact resitivity. This level of resistance is about ten times higher than the ohmic contact to p-type material. Therefore, a pn junction-based IMPATT appears to be the most promising structure due to its lower overall resistivity.

D. Conclusions

For the first time, positive gain has been observed for a SiC transistor at

microwave frequencies. These devices were 6H-SiC MESFETs that had submicron gate lengths and 1 mm gate widths. The highest values for F_t and F_{max} were 2.9 GHz and 1.9 GHz, respectively. The highest current gain and power gain observed at 1.0 GHz were 8.5 dB and 7.0 dB, respectively. Modeling shows that these devices should operate, with high power densities, at frequencies up to 10 GHz. The major issues now are to minimize the same parasitics that have to be dealt with in any high frequency device in any material, primarily gate resistance and source resistance. The gate resistance was the major factor limiting the high frequency operation of the MESFETs. Ideally, this resistance should be reduced by a factor of at least four (<10 Ω) to obtain positive gain at 10 GHz. The issue of source resistance is also important and should be reduced by a factor of two, which will allow both higher power and higher frequency devices.

Avalanche characteristics for a 6H-SiC IMPATT diode have been observed for the first time using a "high-low" doping structure. These Schottky based devices showed avalanche power densities as high as 29 kW/cm^2. While the pn junction based IMPATTs did not show good avalanche characteristics because of inaccuracy in doping and/or thickness, they did show very low reverse bias leakage currents at 200 V. Thus, it is assumed that with the proper doping and thickness, very good avalanche charcteristics will be achieved at about 100 V using this pn junction structure. From the Schottky diode results, it was determined that the contact resistivity of the Schottky contact in forward bias was in the range of 8×10^{-4} Ω-cm^2. This value is too high for high power operation at 60 GHz, the intended frequency for these IMPATT diodes. Since the contact resistivity is much less for an ohmic p-type contact, the pn junction based IMPATT appears to be the most promising structure.

E. Future Research Plans/Goals

Further efforts on the 6H-SiC MESFETs will concentrate on further reducing the parasitic gate resistance via thicker metal overlayers. Several methods will be investigated. A different metal with a lower resistivity (silver) will be tried as an

overlayer. Thicker (>1 μm) self-aligned layers will be attempted, and larger cross-sectional area overlayers (mushroom gates) will be investigated.

The issue of source resistance will also be addressed in several different ways. The first is to continue optimizing the doping and thickness of the present structure to achieve lower source resistances. A second method will involve the fabrication of recessed gates, a method by which the channel layer is only thinned directly below the gate, keeping the source-gate cross-sectional area much larger. If this can be achieved, it will have a large effect on the high frequency behavior of these devices. Thirdly, some MESFETs will be attempted on β-SiC thin films. Some recent breakthroughs at Cree Research have resulted in very high quality 1 inch diameter β-SiC thin films. The higher electron mobility of β-SiC will allow a very significant decrease in source resistance. As such, films are being grown and characterized for use in high frequency MESFET structures.

Future IMPATT diodes will focus on the fabrication of pn junction "high-low" structures. Some new modeling efforts will probably be required to determine the exact doping and thickness that is required for good avalanche characteristics and 60 GHz operation. These devices will then be fabricated and measured.

IV. Characterization of Ti Films on Alpha (6H)-SiC (Spellman/Davis–NCSU)

A. Overview

The future development of SiC device technology depends on, and may in fact be limited by, the ability to form good ohmic and Schottky contacts. In the past metal contacts have been chosen for study to a large extent based on empirical approaches. This study approaches the problem from both the theoretical and the experimental points of view in the hopes of finding superior ohmic and Schottky contacts to 6H-SiC. The polytype 6H-SiC has been chosen for this study due to the ability to grow bulk crystals and thin films which have low defect densities [1].

For an ideal, abrupt junction the barrier height is defined by the Schottky-Mott

limit, or the difference between the metal work function and the electron affinity of the semiconductor. However, interface states and chemical reactions between the metal and semiconductor cause deviations from ideality. In fact, Pelletier *et al.* [2] have reported Fermi level pinning in 6H-SiC due to intrinsic surface states, indicating little dependence of barrier height on the work function of the metal, which has often been the case in practice. On the other hand, Waldrop *et al.* [3] have reported strong work function dependence for metal/β-SiC barrier heights, giving encouragement for the ability to control barrier heights of metals on 6H-SiC.

Based on work functions and equilibrium phase diagrams with Si and C, six metals have been chosen for this study; these include Pt and Se for rectifying contacts and Ti, Hf, Sr, and Co for potential ohmic contacts. In consideration of barrier heights, these metals were chosen based on the theory that metals with high work functions should form good rectifying contacts to n-type SiC, while metals with low work functions are desired for ohmic contacts.

However, the significance of the chemistry between the materials must not be underemphasized; in fact, interfacial reactions could result in one phase dominating the electrical characteristics of the contact. Hence, it may be possible to attribute ohmic or Schottky behavior to a particular silicide, carbide, or ternary phase. Recent work by W. T. Petuskey at Arizona State University, showing the possible stable phases in the Ti/SiC system, has made Ti even more attractive to study as a contact.

This report will discuss the characterization of Ti deposited on (0001) 6H-SiC, which was found to be epitaxial. The epitaxial growth of Ti not only results in better film quality, but it opens up possibilities for growing multilayers for device applications.

B. Experimental Procedure

The substrates used in this study are 6H-SiC wafers provided by Cree Research, Inc. The wafers are 1" in diameter and are nitrogen doped n-type ($\sim 5 \times 10^{17}/cm^3$). All growth and analyses were done on the Si terminated face,

represented as (0001). In certain cases an epitaxial layer (~0.5 μm) of 6H-SiC of improved quality was grown on the substrate surface. These layers were also nitrogen doped n-type (~$10^{18}/cm^3$).

Modifications in surface preparation have been made in the process of trying to determine the optimum cleaning technique. These *ex-situ* cleaning techniques consisted of an RCA clean [10 min. in (5:1:1) $H_2O/H_2O_2/NH_4OH$, 5 min. water rinse, 10 min. in (5:1:1) $H_2O/H_2O_2/HCl$, and an additional 5 min. water rinse] and/or and oxide etch. After finding high fluorine concentrations left after a 49% HF etch, a modified etchant which consisted of ethanol/deionized water/HF (10:1:1) was used [4].

Chemical analysis with x-ray photoelectron spectroscopy indicate the need for an *in-situ* cleaning technique. In the most recent experiments substrates were exposed to an *in-situ* remote hydrogen plasma immediately after etching with the ethanol/DI water/HF mixture. The plasma operated at 20 W consisted of H_2 at 5 sccm in a He diluent at 30 sccm. The substrate, which contained an epilayer, was maintained at 200°C throughout the 10 min. discharge. Ti was subsequently evaporated from a hot wire filament in UHV onto the SiC surface, which was at room temperature. Low energy electron diffraction (LEED) photographs taken before and after cleaning and after deposition will be presented in a subsequent section.

In the remainder of the reported experiments, Ti was either evaporated by electron beam or thermally evaporated from a hot wire filament. In all cases except the one involving TEM analysis, the substrates were kept at room temperature. All annealing steps were performed *in-situ* under UHV.

A TEM specimen was prepared in cross-section and examined with both a Hitachi 800 and a JEOL 200CX for high resolution TEM. Other microstructural information was obtained by J. Posthill at Research Triangle Institute from Rutherford Backscattering (2 MeV He+ ions). Current-voltage measurements were taken with an HP 4145A Semiconductor Parameter Analyzer. *In-situ* monitoring was made possible with retarding LEED/Auger.

C. Results

The first indication of epitaxial growth of Ti was provided by LEED after evaporation from a hot wire filament onto (0001) SiC at room temperature. The LEED pattern taken of the 'clean' SiC surface before Ti deposition showed a bulk 1×1 pattern, indicative of no surface reconstruction. After deposition the LEED pattern did not change, and in fact remained unchanged throughout annealing to 900°C. (Figure 25 shows LEED patterns taken before and after Ti deposition onto an epilayer which had been exposed to a remote hydrogen plasma.)

In conjunction with the structural information obtained from LEED, Auger electron spectroscopy (AES) was used as a means of fingerprinting elements in the near-surface region. Figure 17 shows a series of Auger spectra taken both before and after depositing Ti. The amount of oxygen on the surface was below the detection limits of the system. After depositing 100 A of Ti (no anneal), the Si and C peaks disappeared, and 2 peaks characteristic of Ti appeared. A total thickness of 400 A was deposited. After annealing to 500°C or 600°C, the Si and C peaks began to reappear. An interesting result occurred at 800°C; a sharp Si peak appeared, while a smaller carbon peak remained. SEM pictures showed complete coverage of the substrate, but a dimpled topography. In comparison, SEM pictures of a Ti film deposited at room temperature but not annealed showed a smooth topography and complete coverage of the substrate.

RBS was also used to compare the annealed and non-annealed films and to obtain structural information. Figure 18 shows the backscattering yield from both the substrate and the non-annealed Ti film. The corresponding spectra for the annealed sample is shown in Figure 19. By aligning the SiC substrate such that the incoming He+ ions channel through rather than become backscattered, the percent crystallinity can be quantified by the parameter χ, which is the ratio of the aligned to the non-aligned spectrum. A value of χ=0 corresponds to 100% crystallinity. The non-annealed Ti film was found to have a χ value of 0.71, while χ was calculated to be 0.74 for the annealed Ti.

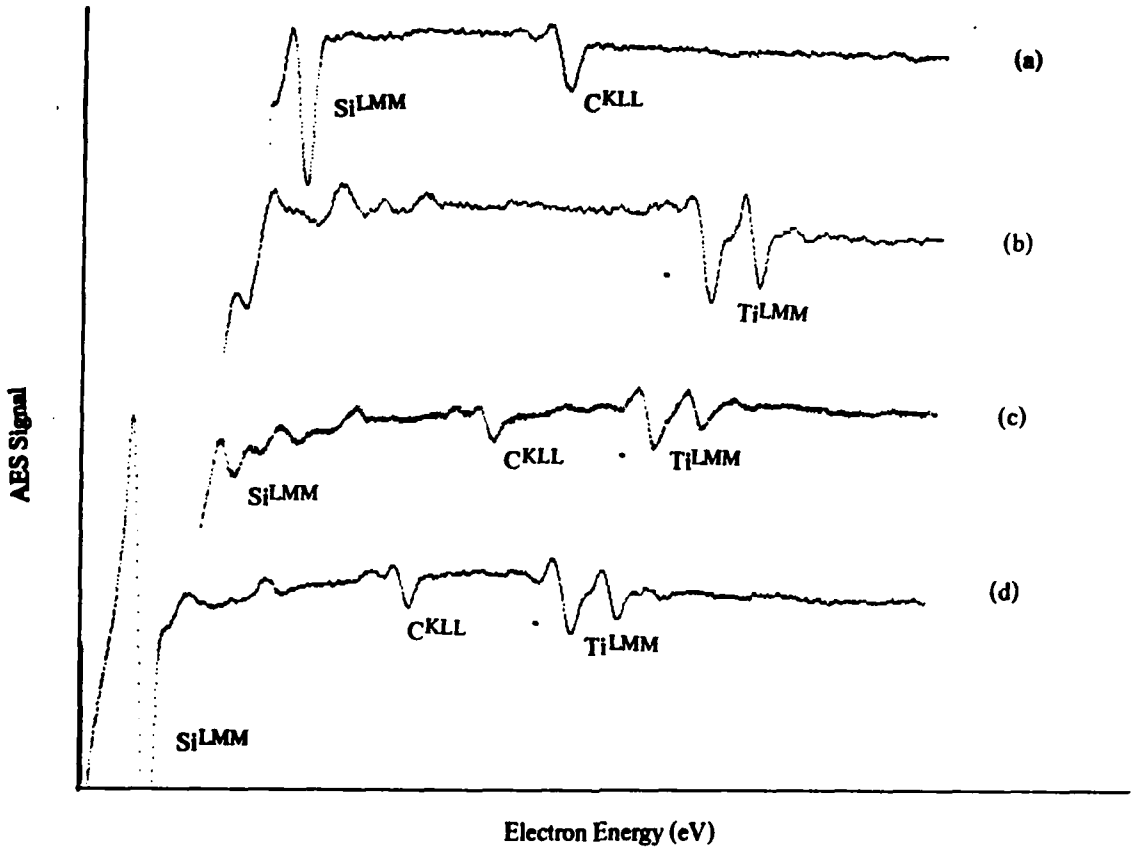

Figure 17. Auger spectra of (a) 6H-SiC (0001) surface, (b) 200 A Ti on SiC (as-deposited at room temperature), (c) 200 A Ti on SiC (annealed to 600°C), and (d) 200 A Ti on SiC (annealed to 800°C).

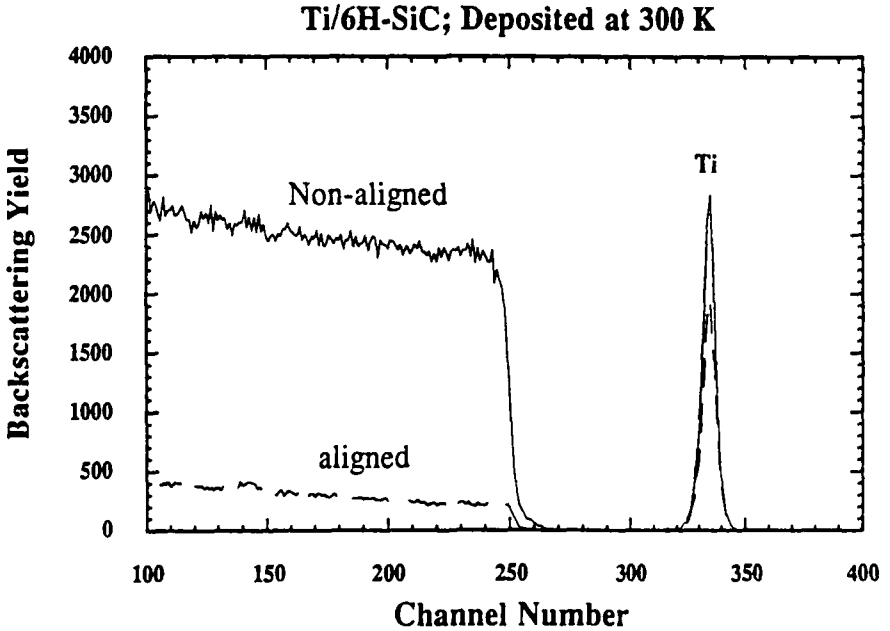

Figure 18. RBS spectra for 400 A Ti deposited on 6H-SiC at room temperature; no anneal.

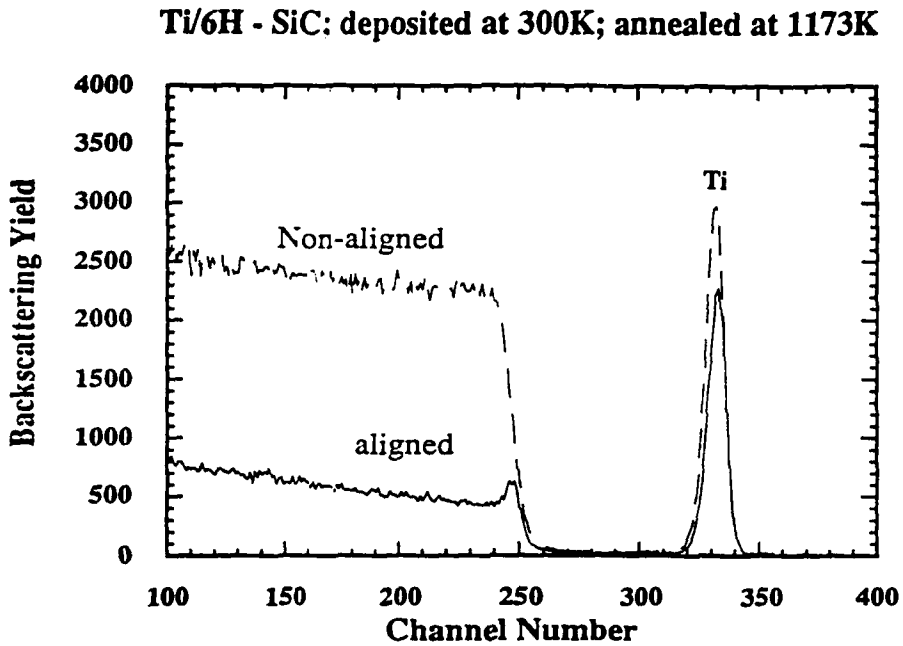

Figure 19. RBS spectra for 500 A Ti deposited on 6H-SiC at room temperature; annealed to 900°C in 100°C steps, 10 min. at each step.

RBS can also be used to identify chemical compounds from bond strength considerations. Figure 20 fingerprints TiC, Ti_xSi_y and Si at the surface after annealing the film at 900°C.

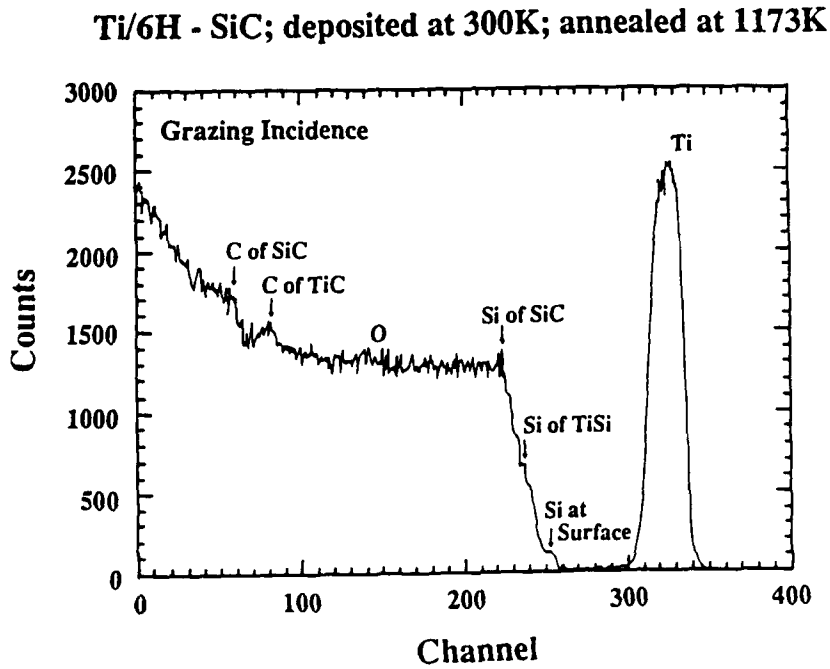

Figure 20. RBS compound identification of Ti deposited on (0001) SiC at room temperature and annealed to 900°C.

Current-voltage measurements were taken both as a means to characterize the electrical properties of the contacts and to monitor possible changes in the interface chemistry with annealing. Figure 21 shows how annealing at relatively low temperature can alter the electrical characteristics significantly. On annealing the contact at 400°C for 50 min., the contact starts to resemble ohmic-like behavior.

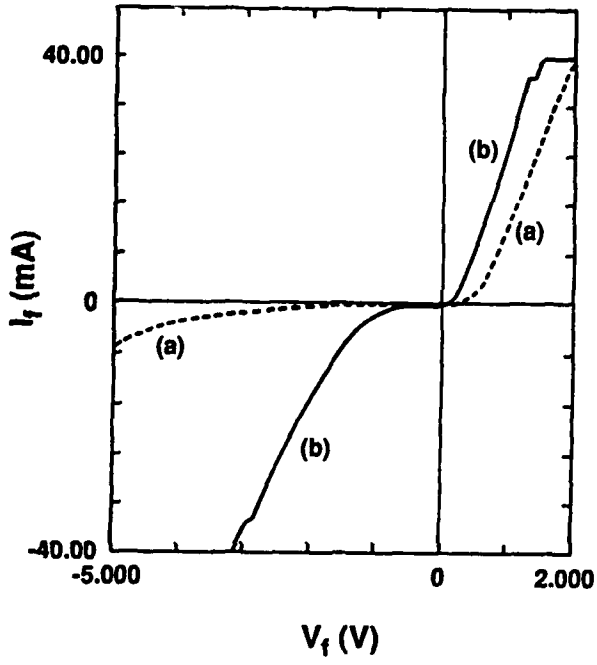

Figure 21. Current-voltage measurements of 100 mil diameter Ti contact diodes on 6H-SiC (a) deposited at room temperature; no anneal and (b) deposited at room temperature; annealed at 400°C for 50 min.

Selected area diffraction patterns taken in XTEM (Figure 22) were taken for two different orientations of the SiC substrate [5] with both the deposited film and the substrate contributing to each pattern. Spots to the outside of nearby spots in the pattern originate from the deposited film. These 'extra' spots indicate that the film has the hexagonal closed packed structure of Ti in the same orientation as the substrate.

The XTEM micrograph in Figure 23 shows the same Ti films to be of relatively good quality, but with threading dislocations to relieve a 4% lattice mismatch strain between the film and substrate. The interface is more clearly represented under high resolution (Figure 24), although there is some ambiguity in defining an abrupt interface.

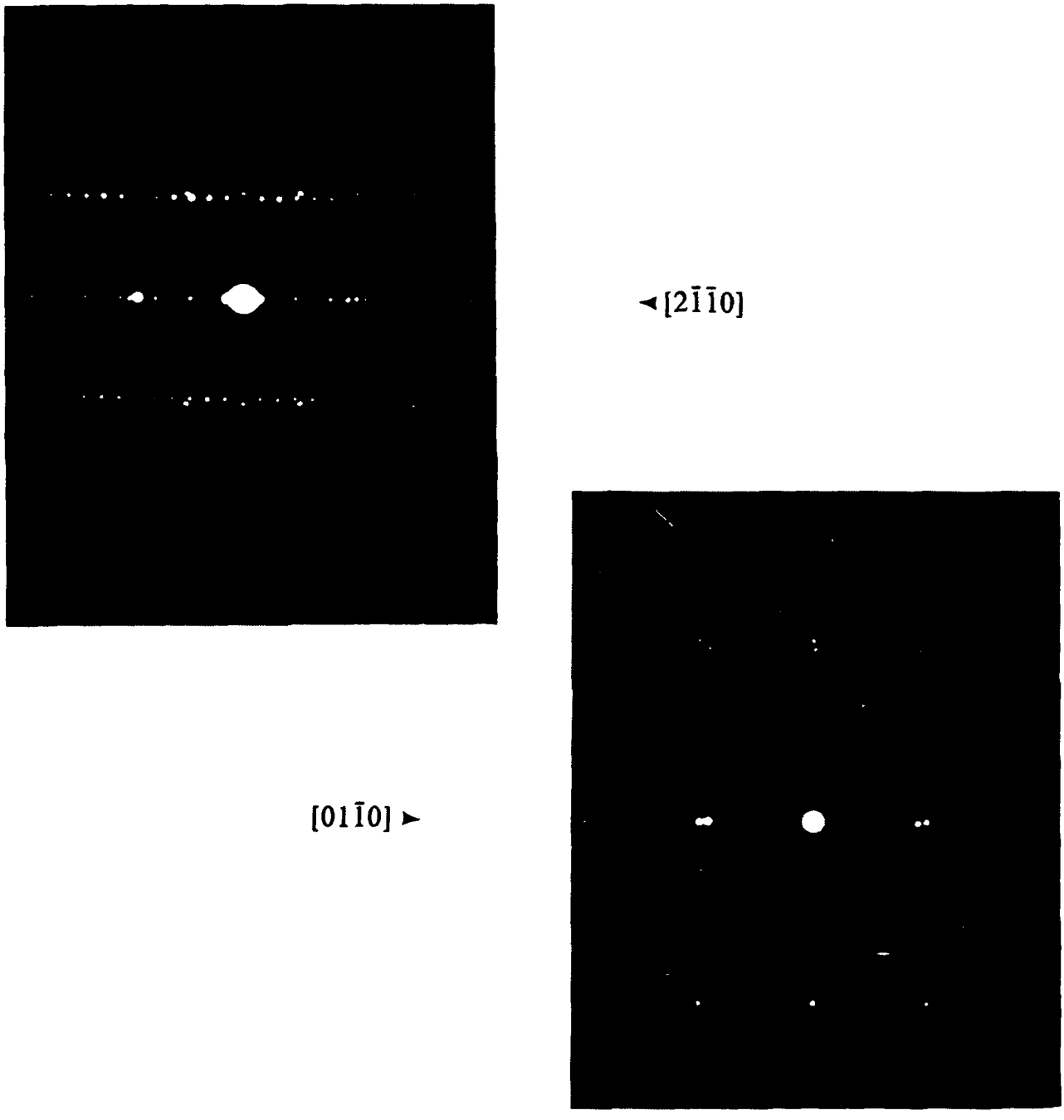

Figure 22. Selected area diffraction patterns of Ti /6H-SiC; deposited at 400 °C; electron beam evaporation; film thickness: 900 A. (Hitachi 800)

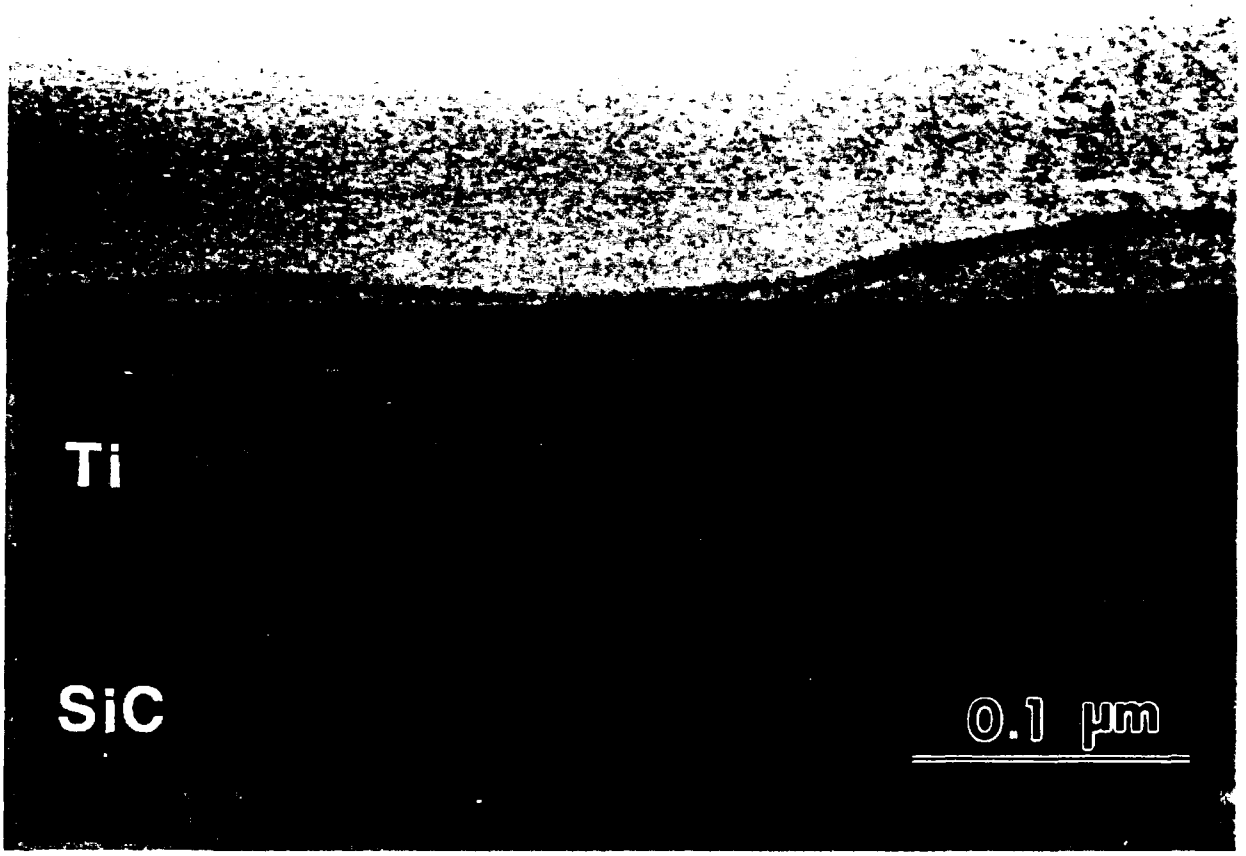

Figure 23. XTEM micrograph of Ti deposited on 6H-SiC at 400 °C; electron beam evaporation; film thickness: 900 A. (Hitachi 800)

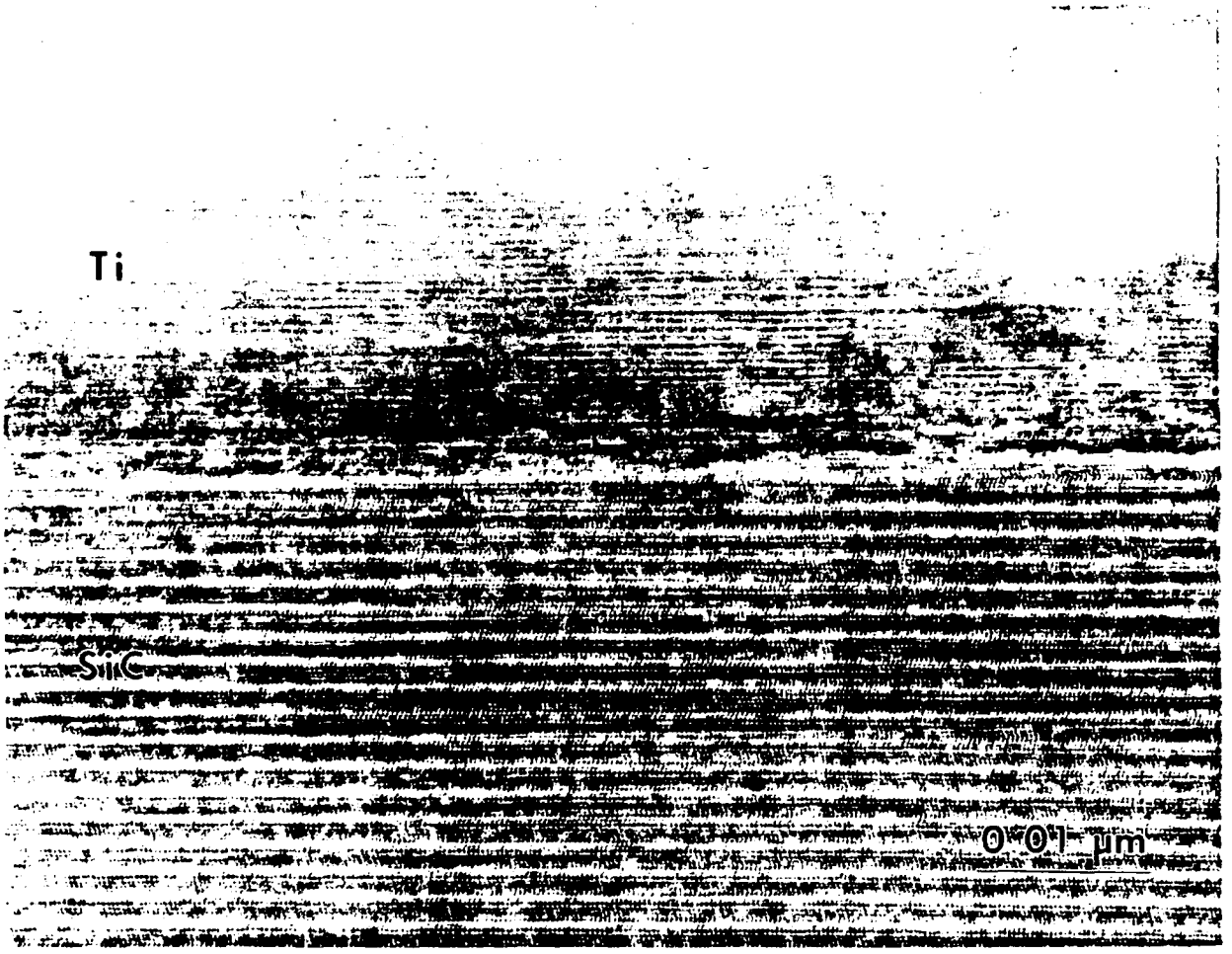

Figure 24. HRTEM micrograph of Ti deposited on 6H-SiC at 400 °C; electron beam evaporation; film thickness: 900 A. (JEOL 200CX)

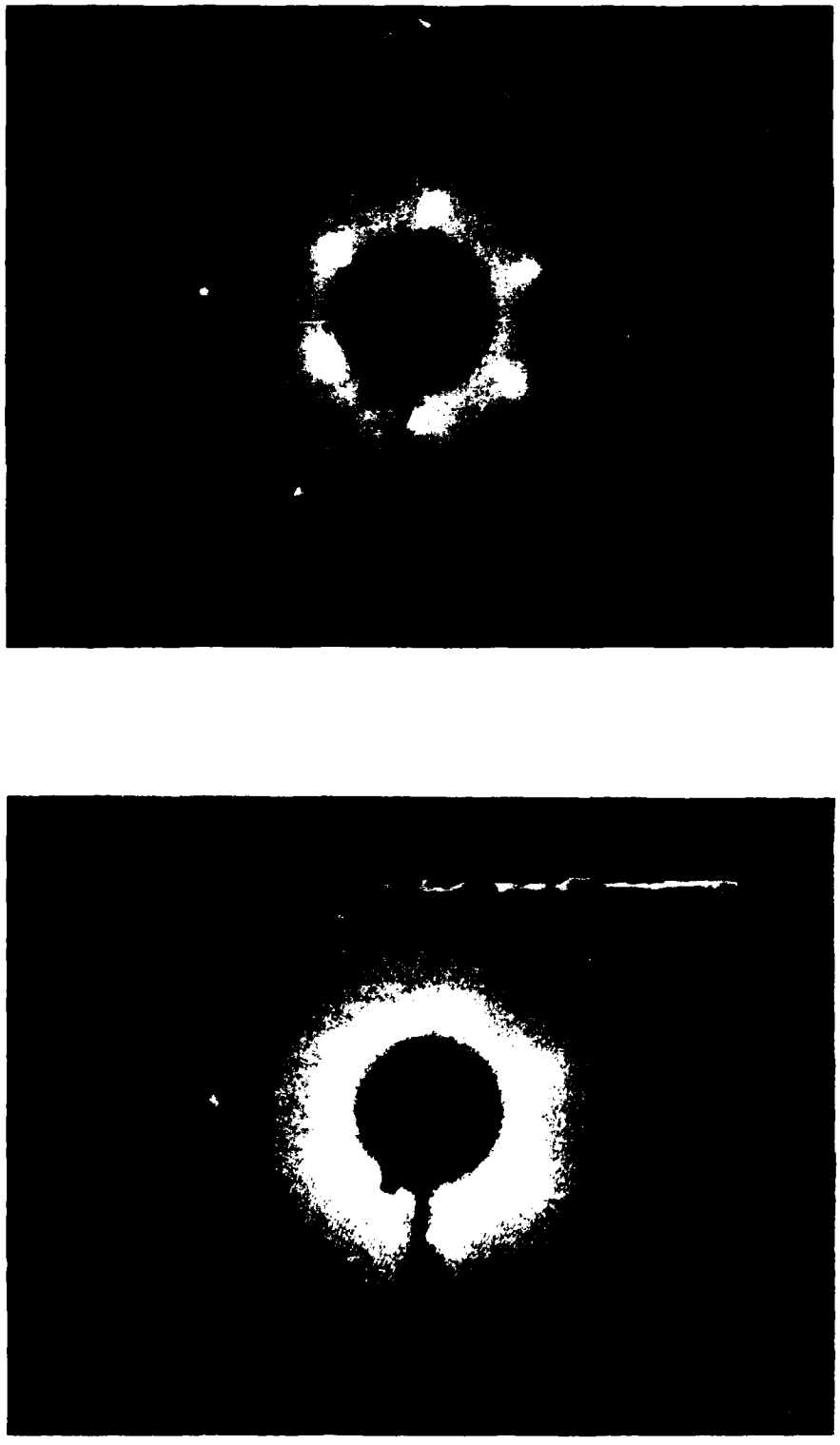

Figure 25. LEED patterns with beam energy 80 eV of (a) (0001) SiC epilayer etched for 10 min. in ethanol/H_2O/HF (10:1:1) and (b) after remote hydrogen plasma clean and

(c) after 100 A Ti deposition at room temperature

Low energy electron diffraction patterns were taken of an epitaxial SiC layer before and after exposure to a remote hydrogen plasma (Figure 25a, b). The spots were observed to become sharper after cleaning. Auger spectra were also taken but did not give meaningful results due to vibrations from non-isolated vacuum pumps. In the immediate future it is hoped that ultraviolet photoelectron spectroscopy (UPS) will characterize the chemical state of the substrate surface.

Figure 25 shows a LEED pattern taken after depositing 100 A Ti at room temperature. The spreading out of the spots is attributed to an increased distance between the LEED source and the sample. Although the spots look to be slightly more diffuse, the pattern shows the same 1×1 pattern of the bulk SiC.

D. Discussion

The combination of analyses with LEED, TEM, and RBS indicate epitaxial growth of Ti on (0001) SiC at both room temperature and 400°C. This result is not surprising after comparing the crystal structures of each of the materials separately.

The substrates have a hexagonal crystal structure with lattice parameter a = 3.08 A. The crystal structure of Ti is also hexagonal with a = 2.95 A. This difference in lattice parameters corresponds to only a 4% lattice mismatch. Similar results are predicted for hafnium, its crystal structure (hexagonal, a = 3.19 A), corresponding to less than 4% mismatch with 6H-SiC.

In addition, the crystal structure at the surface of a 400 A Ti film remained the same through a 900°C anneal even though the Auger data (Figure 17) show a change in surface composition. The absence of islands in the SEM pictures indicate that the Si and C peaks originate from the near surface region of the film rather than from the substrate itself. Bellina *et al.* [6] suggest the formation of TiC at Ti/3C-SiC interfaces and diffusion of Si to the surface, which agrees quite well with the RBS data in Figure 20.

A comparison of the chemical information obtained from this RBS data with the TEM studies of a film deposited at 400°C suggests that the kinetics at 400°C are too slow to result in significant interfacial compound formation. Selected area diffraction patterns (Figure 22) show that the film has the hexagonal crystal structure of Ti; any interfacial reactions, which would give rise to additional spots in the diffraction pattern (e.g. TiC has NaCl crystal structure), must be confined to a very small region. Because the chemical kinetics at 800°C are quite fast, we have chosen to begin a detailed study of the interrelation of the chemical, microstructural, and electrical characteristics on annealing at 700°C.

Encouraging data regarding the formation of an ohmic contact after annealing at 700°C is provided by current-voltage measurements. Figure 21 shows a significant shift towards ohmic behavior after annealing at relatively low temperature (400°C for 50 min.). Electrical measurements (current-voltage and internal photoemission) of a time series anneal at 700°C will be correlated with chemical and microstructural analyses primarily by TEM and RBS.

A recent thrust of this project has been to use a remote hydrogen plasma to strip the substrate surface of any oxides and hydrocarbons prior to depositing the

metal. Because the plasma is remote, physical damage to the substrate surface is minimized. LEED patterns taken after cleaning show the same bulk 1×1 pattern of the surface before cleaning (Figure 25a, b). However, the spots were observed to become sharper after cleaning, probably due to the removal of surface contaminants. The LEED data will need to be correlated with a chemical analysis technique (Auger or UPS) to get a clear picture of the state of the surface.

E. Conclusions

Heteroepitaxial growth of TI on (0001) 6H-SiC has been observed and characterized for both room temperature and elevated temperature deposition. Current-voltage measurements display shifts toward ohmic behavior after annealing at 400°C for 50 min. Rbs data shows the presence of TiC, Ti_xSi_y, and surface Si in the deposited film after annealing at 900°F.

In the immediate future a time series anneal of Ti/6H-SiC at 700°C will be characterized chemically and microstructurally and correlated with electrical characteristics. Samples have been and will be sent for determination of barrier height by internal photoemission. It is hoped that desirable electrical behavior of the contact can be attributed to the formation of a particular compound at the interface. If ohmic behavior is found, a transmission line model (TLM) mask has been fabricated and will be used to measure contact resistance.

Many of the processes which have been developed for studying Ti/SiC contacts will be used for studying five other metals selected for this research. These metals include Pt and Se for rectifying and Co, Sr, and Hf as potential ohmic contacts.

V. Gas-Source Molecular Beam Epitaxy of SiC (Rowland/Davis–NCSU)

A. Overview

A system designed for low temperature growth of low defect-density monocrystalline SiC films by gas-source molecular beam epitaxy is virtually

completed. The technique of molecular beam epitaxy (MBE) allows for precise control of growth parameters and minimization of sample contamination during deposition due to the ultra-high vacuum nature of the process. Parameters such as growth thickness and dopant concentration can thus be controlled as closely as possible and reproducibly obtained using this technique. Gaseous species will be provided to the sample surface using a pressure-controlled flow system. This deposition system will be used for low temperature growth and doping of monocrystalline SiC thin films.

B. Experimental Procedure

Growth System. A schematic of the system to be used for gas-source MBE is shown in Figure 26. Samples are first introduced into a small load lock chamber, the load lock chamber is evacuated, and samples are then transferred to the heating stage in the growth chamber. The load lock is used in order to increase sample throughput, as well as to keep the main deposition chamber under vacuum while samples are exchanged. It is pumped by a Balzers TPU 060 turbomolecular pump backed by a Sargent-Welch rotary vane pump. The load lock is operational, and pressures of 1×10^{-6} torr or below are easily reached in 30 minutes, at which point samples are transferred to the growth chamber.

The growth chamber will be utilized for both sample cleaning and deposition. Substrates will be cleaned prior to deposition by using an Ar^+ plasma to produce H^+ radicals from H_2 introduced into the system downstream from the plasma. The Ar^+ plasma will be obtained using an electron cyclotron resonance (ECR) plasma source developed in our laboratory [7]. This source is now installed, and will be characterized in the near future. To date, no published work has been performed on plasma cleaning of α–SiC, but some results using an rf plasma system are contained in a previous section of this report.

Samples will be heated using a heater specially designed for this system. Heat is produced by resistive heating of a coiled tungsten filament within a SiC-coated graphite cylindrical heating cavity lined with molybdenum and tungsten heat shielding.

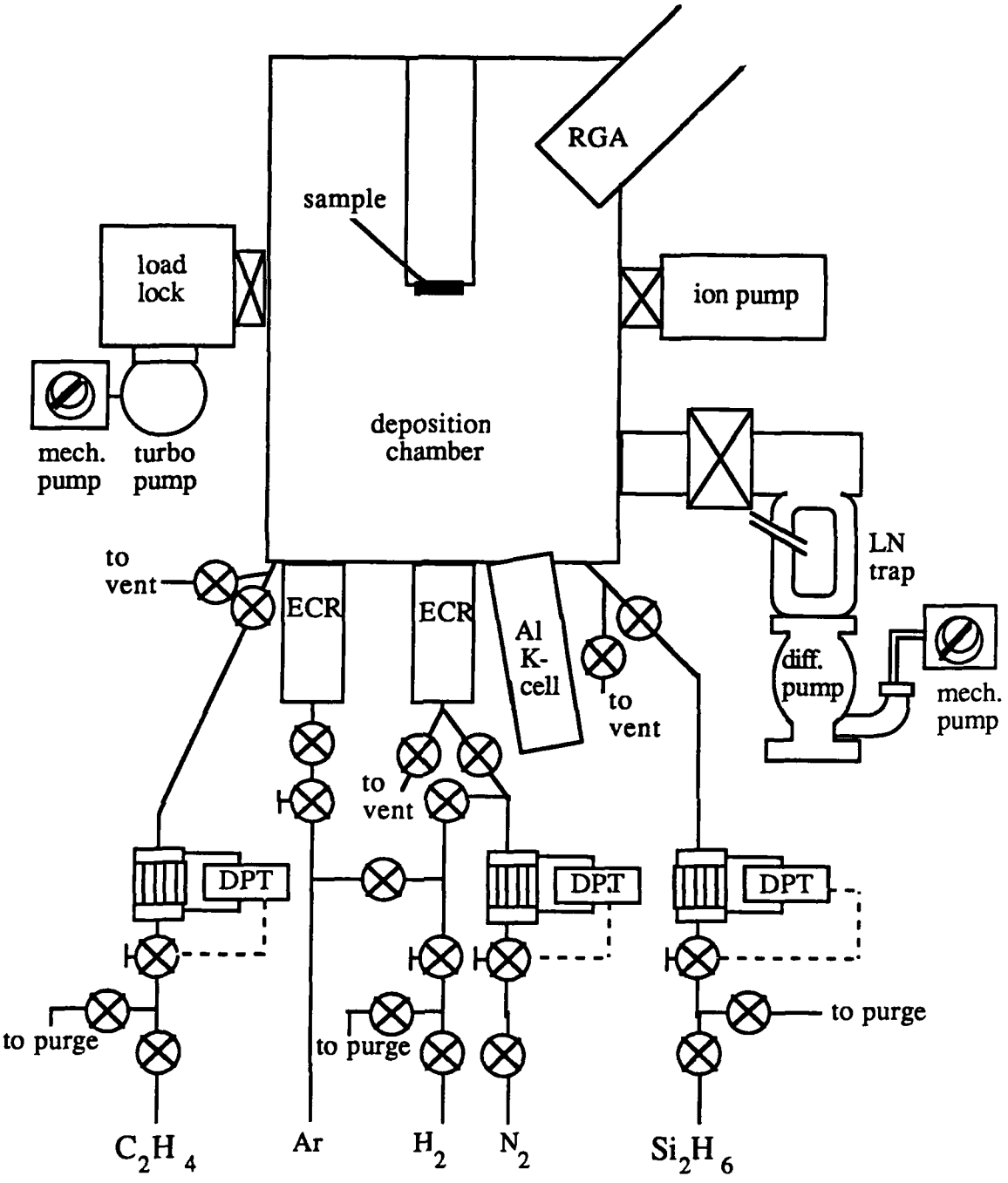

Figure 26: Schematic of molecular beam epitaxy system.

A high-purity pyrolitic BN disk is used as an insulating plate for holding the W coil in place. The sample is shielded from line-of-sight interactions from all parts of the heater not coated with SiC to minimize sample contamination. The heater shall be capable of temperatures of over 1000°C. Samples will also be rotated during growth to ensure sample uniformity.

Species used in growth are introduced by way of the source flange. The source flange is equipped with ports for up to five solid sources and five gaseous sources. Disilane (Si_2H_6) will be used as a source of silicon, and will be supplied through a pressure-controlled flow system described in the next section. Ethylene (C_2H_4) will be used as a source of carbon. It will be introduced through a specially designed ECR plasma source. This source will enable the introduction of ethylene downstream of an ECR-induced Ar^+ plasma. Aluminum will be provided by a solid-source MBE effusion cell made by EPI Systems. Diatomic nitrogen (N_2) decomposed with an ECR source will be used as a source of nitrogen. Mechanical air-actuated shutters will be used with all sources to aid rapid switching between sources for abrupt doping profiles.

In the case of MBE, the distance between collisions for each molecule is much longer than the dimensions of the deposition chamber. This implies that flow is in the molecular regime, and flow rates are too low for standard mass flow controllers. Gas mixtures can be used, but their use would compromise source purity and control. A method of flow measurement and control has been developed which works very well in the molecular regime [8]. It is based on the fact that in molecular flow, the

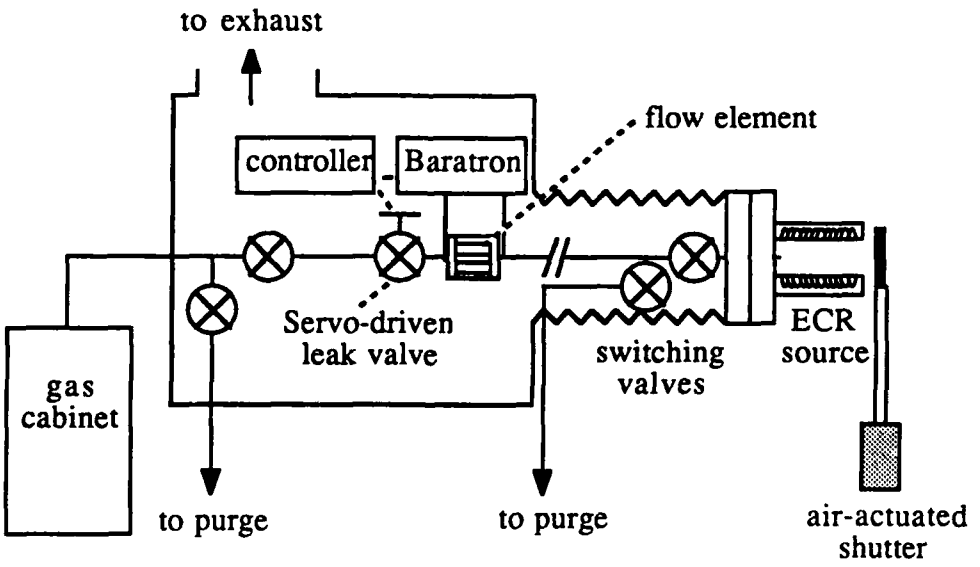

Figure 27. Valve system for gaseous sources.

conductance of a tube is not a function of pressure. The mass flow, Q, through an element can be expressed as

$$Q = C\Delta P$$

where ΔP is the pressure difference and C is the conductance. The conductance of a cylindrical tube or series of cylindrical tubes in molecular flow can be accurately calculated. If the pressure difference across this element of known conductance is measured, then the flow rate through this element can be easily found. The equipment used consists of a MKS CFE-0.5 precision molecular flow element, a MKS Model 120 differential capacitance manometer to measure the pressure difference across the element, and a Granville-Phillips Model 216 servo-driven leak valve and controller to control the gas flow to the element. The gas flow control system configuration is shown in Figure 27. Each gas used has its own flow control system. The entire flow control system, from the gas cabinet to the deposition chamber, will be exhausted for safety considerations. This type of system has been shown to enable the precise control of gas flow in the molecular regime, and can switch gases on in about 1 second and off in about 2 to 4 seconds [9].

The chamber also contains a UTI-100C mass spectrometer, which will be used in order to determine species present during growth. Characterization of films using RHEED during growth is also planned. The system is pumped using a Varian VHS-6 2400 l/s diffusion pump with a Vacuum Generators UHV-quality liquid nitrogen cold trap backed by a rotary vane pump. A Perkin-Elmer ion pump has also been installed to help achieve UHV base pressures prior to deposition. Background pressures in the low 10^{-10} torr range are obtainable in this system.

Deposition Procedures. Growth of SiC films will take place on sublimation-grown, 1-inch diameter {0001} single-crystal 6H-SiC substrates provided by Cree Research. These samples shall by nature of the growth process and the subsequent cutting into wafer form, have some off-axis component. Previous results suggest that films grown on off-axis 6H-SiC substrates will be 6H-SiC [10,11]. Thus, growth on

these samples is expected to be of the 6H polytype.

Immediately prior to introduction to the growth system, the oxide layer on each sample shall be removed by an HF acid solution. Samples will then be introduced into the growth chamber by way of the load lock. Samples will be cleaned *in situ* by the introduction of H_2 downstream from a ECR-induced remote Ar^+ plasma. Substrates will be heated to 473-673K for this cleaning step. Both Ar and H_2 will be introduced in to the system by manual leak valves. Growth will be performed in the system described in the previous section.

Although growth of SiC is the primary goal of this research, growth of Si and C shall be performed initially on 1-inch (100) Si substrates in order to optimize system and source parameters using a simpler materials system than SiC. Si samples will be plasma cleaned using the method described above. Growth of Si will be performed at 873-1173K using disilane (Si_2H_6) introduced via the flow system described in the previous section. Flow rates of Si_2H_6 used to find optimum growth conditions shall be 0.5-5 sccm. Layer thickness obtained shall be 0.01-5 μm. Growth of thin (10-15 nm) layers of C on Si using downstream decomposition of C_2H_4. Flow rates of C_2H_4 and Ar shall be 0.5-5 sccm and 1-10 sccm respectively. C_2H_4 shall be introduced using the pressure-controlled flow system. Ar will be introduced using a manual leak valve. Previous results show that under certain conditions the deposited C combines with Si from the substrate to form a thin SiC layer [12]. Conditions necessary for this to occur in this MBE system will be found. In previous growth of 3C-SiC on Si performed in our laboratory, temperatures necessary to form this buffer layer were 1660K [13]. Surface morphology of grown films will be examined using optical microscopy. In addition, films with the smoothest surface morphology will be further examined using cross-sectional transmission electron microscopy (XTEM) and plan-view TEM.

Growth of SiC thin films will be performed using Si_2H_6 and C_2H_4 introduced as described in the previous section. Experimental flow rates of Si_2H_6 and C_2H_4 shall be in the 0.5-5 sccm range for SiC deposition. Empirical experiments will commence to

find the proper growth temperature and flow rates of the SiC growth species. Growth temperatures to be used will be in the 1273-1673K range. Chemical vapor deposition (CVD) research conducted in our laboratory found an optimum growth temperature of 1773K [10,11], but growth species were not decomposed by other means prior to reaching the substrate. Doping experiments will begin once growth conditions for monocrystalline SiC growth have been optimized. Dopants to be used in this research are Al obtained from a standard MBE effusion cell and N obtained by decomposition of N_2 in an ECR plasma. Flow rates used will be from 10^{-3} to 1 sccm.

Surface morphology of grown films will be examined using Nomarski optical microscopy and scanning electron microscopy. On those films with the best surface morphology, samples for XTEM and plan-view TEM will be prepared. TEM with electron diffraction will be used to examine the SiC film as well as the substrate/film interface. In addition, dopant concentration profiles as well as concentrations of residual impurities will be obtained using secondary ion mass spectrometry (SIMS). Once growth conditions have been optimized, undoped and doped samples will be electrically characterized. Current-voltage characteristics will be obtained from Au Schottky diodes. These will be formed by evaporating Au on lithographically patterned samples. The samples will be patterned so that large-area Au contacts will be also used as the ohmic contact and smaller Au dots will be used as the rectifying contact. In addition, a mercury probe will be used to determine carrier type and concentration.

C. Discussion

High-quality monocrystalline growth of SiC is historically quite difficult and takes place only at very high temperatures. The difficulty in obtaining high-quality single crystal SiC films seems to have been overcome due to recent developments in 6H-SiC bulk crystal growth at Cree Research resulting in the availability of 6H-SiC substrates for homoepitaxial growth. However, many problems remain including the inherent n-type character of "undoped" films, the difficulty in *in situ* doping of films, especially at lower concentrations, and the materials-related difficulties of film

deposition at temperatures as high as those currently used for SiC growth. As a result, this system was brought into existence to address these problems.

In order to minimize impurity incorporation, the system will achieve base pressures in the UHV regime prior to deposition. All sources used will be the highest purity available. Samples during growth sit at an 45° tilt from upside down in order that particles from the system cannot fall on the sample, as well as ensuring that deposition that inadvertently occurs on the outer portion of the sample heater assembly cannot flake off into sources contained within the source flange. The valve system was designed to enable reproducible doping down to extremely low levels. MBE effusion cells are capable of providing source fluxes much lower than will be used in this research. In addition, flow rates of N_2 as low as 5×10^{-4} sccm are possible to reproducibly obtain using this valve system.

The primary obstacle to low-temperature growth of SiC is the difficulty in locating a suitable source for monomolecular carbon. Several methods for the deposition of solid carbon have been considered, and shall be discussed below. The most promising of these is resistive heating of a graphite filament [13]. If the filament is heated to around 2500°C, a significant flux of carbon leaves the sample due to thermal evaporation. The majority of C leaving the filament has been shown to be monomolecular in nature. This method has been utilized for carbon doping of GaAs in an MBE system. Huge amounts of power and a filament with very large cross-section would be necessary in order to obtain a flux sufficient for MBE growth of a binary carbide such as SiC. This fact precludes the use of this method at this time in this project. Other potential methods for solid-source deposition of C, such as laser evaporation and electron-beam evaporation, do not as yet yield large percentages of monomolecular carbon.

Gaseous sources of carbon such as hydrocarbons are relatively difficult to decompose. The growth temperature of SiC can be substantially lowered if the energy required for this decomposition can be decreased. One method which is useful in some

instances is laser decomposition. High-energy monochromatic light, such as that produced by a laser, can impart sufficient energy to gaseous molecules to decompose them. Laser-enhanced chemical vapor deposition is a well-known technique for obtaining lower-temperature growth of many materials at pressures near one atmosphere. However, the efficiency of the decomposition process in the pressure range used in this research is extremely low.

Plasma decomposition is a proven method for low-temperature decomposition of gaseous species. The feasibility of an ECR source for monocrystalline growth of various materials in an MBE environment has been demonstrated [14,15]. Decomposition of ethylene will utilize a previously mentioned NCSU-developed ECR source modified to allow the downstream introduction of a gaseous species. Downstream introduction of a carbon-containing species is necessary because of the electrically conducting nature of carbon deposits on the inside of the microwave cavity. Argon gas will be used to sustain the plasma. Valves will be placed as close to the source as possible to minimize dead space and maximize control of the ethylene supply.

D. Conclusions

A system for growth of monocrystalline SiC thin films using gas-source MBE has been designed and is virtually completed. This system consists of a loading chamber and a deposition/cleaning chamber. The deposition chamber has the capability of using both solid and gaseous sources, and both will be used in this research. Gas flow will be controlled using a flow system based on measurement of the pressure drop across an element of constant conductance.

Samples will be cleaned prior to deposition using H^+ introduced downstream of an Ar^+ electron cyclotron resonance-induced plasma. 6H-SiC growth will occur on 6H-SiC substrates provided by Cree Research, Inc. Silicon will be provided by thermal decomposition of disilane. Ethylene will be decomposed to an activated carbon-containing species using an electron cyclotron resonance plasma. Dopants for this

research will be nitrogen decomposed using an ECR plasma and Al from an MBE effusion cell. Initial growth experiments will consist of growth of Si and buffer layers of SiC on Si substrates. Growth experiments on SiC will then be performed to optimize growth parameters. *In situ* doping experiments will be performed, and samples grown will be characterized using optical microscopy, SEM, TEM, SIMS, and electrical techniques.

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